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MM&T PROGRAM TO ESTABLISH PRODUCTION TECHNIQUES FOR THE AUTOMATIC DETECTION AND QUALIFICATION OF TRACE ELEMENTS PRESENT IN THE PRODUCTION OF MICROWAVE SEMICONDUCTORS

FIRST QUARTERLY REPORT
23 August 1977 to 23 November 1977

Placed by

Production Division, Procurement and Production Directorate
USAECOM, Fort Monmouth, New Jersey 07703

Contract DAAB07-77-C-0561

Harris Corporation, PRD Electronics Division
6801 Jericho Turnpike, Syosset, New York 11791

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MM&T PROGRAM TO ESTABLISH PRODUCTION TECHNIQUES FOR THE AUTOMATIC DETECTION AND QUALIFICATION OF TRACE ELEMENTS PRESENT IN THE PRODUCTION OF MICROWAVE SEMICONDUCTORS

FIRST QUARTERLY REPORT

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Object of Study

Establish production technique for the automatic detection and concentration quantification of the trace elements (impurities) in the organic and inorganic compounds and solutions that are used in the fabrication of microwave semiconductors and the determination of acceptable impurity levels.

Contract No.: DAAB07-77-C-0561

Report Prepared by: Roy W. Spacie

Appendices A and B prepared by: Dr. George P. Allendorf

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A project was undertaken to improve the yield in the manufacture of microwave semiconductor diodes by establishing the correlation of product yields to the incidence of contaminants in the reagents and solvents used in the manufacturing process and using these data to model the process for optimization of the yield.

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ABSTRACT

This is the first quarterly progress report on an Army-sponsored study which had as its objective the improvement of yields in the manufacture of microwave semiconductor devices. The industry had been experiencing low yields which were attributed to the incursion of trace levels of contaminants during the manufacturing process. The project plan was to develop a computer model of the manufacturing process which would facilitate correlating yields to measurable levels of contaminants present in the various reagents and solvents. Once a representative model has been achieved, it will be used to optimize yields by signaling the advisability of aborting a batch in mid-process if its predicted yield falls below an optimum level.

During the first quarter, a computer-controlled spectrometer capable of measuring trace metals in concentrations as low as 20 parts per billion was procured. The instrument will serve as the principal measuring device with which the quality of the chemicals will be monitored. A high voltage PIN diode (e.g., JANTX-1N5710) was selected as the device on which the study will be based and a computer model of its manufacturing process has been designed.

During the second quarter, a group of experiments will be designed to determine the sensitivity of yield to the presence of trace elements in the reagents and solvents. The necessary computer programs will be prepared and the spectrometer installed. By the beginning of the third quarter all preparations will have been completed for taking experimental data.

GLOSSARY

Analytic Model: a set of equations and/or logic statements, generally implemented on a computer, which quantitatively represents the interrelationships that characterize a given system.

Boule: a pear-shaped mass formed synthetically in a special furnace with the atomic structure of a single crystal.

Epitaxial: having orientation controlled by the crystalline substrate - used of crystals and of the relationship between them and their substrate.

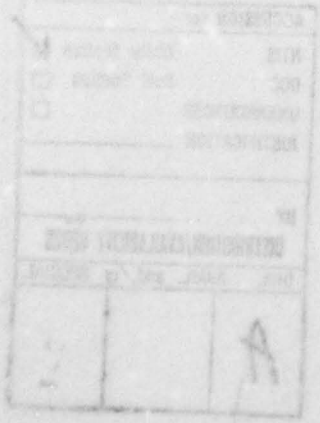
Ionize: to cause a change in the number of electrons in the outer orbits of an atom such that it exhibits a net electrical charge.

Mesa: (~ transistor) structured as a mesa - an isolated hill having steeply sloping sides and a level top.

Nanogram: one billionth of a gram. (Also used are femtogram [one quadrillionth], picogram [one trillionth] and microgram [one millionth].

PIN: (~ diode) an acronym formed from "positive-intrinsic-negative" - a semiconductor device consisting of heavily doped p^+ and n^+ end regions separated by a lightly doped region which can be regarded as intrinsic.

Plasma: a gas in which a significant fraction of its atoms or molecules are ionized.



PURPOSE

The objective of the present Manufacturing Methods and Technology (MM&T) Project is the reduction of microwave semiconductor manufacturing costs through increased product yields. This will be achieved by establishing the correlation between contaminant levels in process materials and their effect upon product yields. These relationships will be used to optimize the manufacturing process toward maximum product yields and minimum unit costs. The project will result in the following developments:

1. An analytical model of the manufacturing process. The model will be implemented in a computer program which will serve as an optimizing control system for the process.

2. A system of batch or lot identification to maintain traceability of contaminants throughout the process, from receiving inspection to the final product.

3. A quantitative chemical analysis system to evaluate contaminants in the materials used in the manufacturing process.

4. A performance specification for an improved manufacturing process control and data management system incorporating these techniques.

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1.1 PROBLEM DESCRIPTION

In the manufacture of microwave semiconductor devices, such as high voltage PIN diodes which are used in military electronic systems, the production yields are very low, typically in the order of 5 to 7 percent. These poor yields are attributed to the inclusion of trace amounts of contaminants within the crystalline structures of the devices. Contaminating elements in the order of a few parts per billion are often sufficient to degrade, if not destroy, the performance of the device. Currently the military is spending $28 million annually for devices of this type. Any improvement in production yields is reflected in lower unit costs. At present usage rates, it is expected that this could represent significant cost savings to the military.

1.2 THE MANUFACTURE OF MICROWAVE SEMICONDUCTOR DEVICES

Typically, the manufacture of microwave semiconductor devices is accomplished as a series of batch processing steps. For example, ultrapure silicon is procured as a raw material. A quantity of this material is melted and recrystallized into a boule. The boule is entered into stock. Sometime later a boule is drawn from stock and sliced into many wafers. The wafers are ground and polished and returned to stock. Small lots of the wafers are drawn from stock as required. The process continues in this manner through 50 to 60 production steps. Similarly, the reagents used in the various process steps are prepared and dispensed in relatively small batches or lots. A single store of partially processed devices may serve as a source for several different product lines.

Because the manufacture of microwave semiconductors is a batch process, it is difficult to maintain traceability of the end product. If an end item should fail to perform properly because of some intrinsic impurity, it is often impossible to trace the impurity back to its source or point of ingress. However, to control impurity levels to a few parts per billion, it is essential that precise traceability be achieved.

Therefore, a fundamental part of the present program must be to devise and implement a system of automatic recordkeeping and data processing so that yields can be correlated with measurable impurity levels at each step of the process.

Table 1-1 is a partial list of those chemical elements known to adversely affect the performance of microwave semiconductor devices. These impurities may enter interstitially into the crystalline structure of the device, enter on a substitutional basis replacing atoms in the normal crystalline matrix, or react chemically with some of the semiconductor materials. In some cases these elemental impurities may migrate to an interface, inducing effects disproportionate to their average concentrations. In most cases, the effects of these impurities upon the electrical performance of the semiconductor device can be predicted with a high degree of accuracy if one knows the concentration of each. Unfortunately, the concentrations of these elements within the semiconductor material can be measured at only a few points in the manufacturing process. Where tests can be made on the semiconductor material they are generally destructive and analytical data must be gathered on a sampling basis.

TABLE 1-1. CRITICAL CONTAMINANTS

Aluminum	Copper	Molybdenum
Antimony	Fluorine	Nickel
Arsenic	Gallium	Oxygen
Bromine	Germanium	Palladium
Boron	Gold	Phosphorus
Cadmium	Iodine	Potassium
Calcium	Iron	Rubidium
Carbon	Lead	Silver
Cesium	Lithium	Sodium
Chlorine	Magnesium	Tin
Chromium	Manganese	Zinc
Cobalt	Mercury	

The chemical impurities may enter the semiconductor material at any of many points in the manufacturing process. They may be induced from the solvents used for cleaning and etching the crystalline wafers, from the materials used in the formation of epitaxial layers, or from the reagents used in any of the 50 to 60 steps of the manufacturing process.

It must be assumed that all of these contaminants are present to a greater or lesser extent in all of the reagents used in the manufacturing process. However, the semiconductor material is not equally susceptible to contamination at each step of the process. For example, the silicon is susceptible to contamination by oxygen only at elevated temperatures. Therefore, it is not sufficient to only know the concentration of these contaminants in each reagent, but one must also know the transfer ratio associated with each element at each step of the process. That is to say, one must know the quantitative relationship between the level of a contaminant in the reagent and the amount of contamination it can be expected to induce into the semiconductor material. Little is known about these transfer ratios at this time. A major task of the present project is to explicitly define the manufacturing process in terms of the interrelationships between the reagents and the semiconductor material and to quantify the transfer ratios of pollutants. Once the ratios are established, it remains to set threshold levels consistent with acceptable yields.

Theoretically, one might analyze the chemical composition of the semiconductor material at each step of the manufacturing process, aborting a batch if it is found to be excessively contaminated. Unfortunately such an approach is neither practical nor economical. The semiconductor material is available for testing at only a relatively few points in the manufacturing process, and where it is available it is in a solid form which does not readily lend itself to chemical analysis. Further, chemical analyses of elements to a few parts per billion are generally extremely expensive and require highly skilled technicians operating with meticulous care. Thus, the costs associated with such an approach would soon outrun any economic gains which may accrue from improved yield. For these reasons, a fundamental part of this program must be to develop a testing program which is capable of providing the necessary control data within the economic constraints of improved yields.

A detailed description of the microwave semiconductor device technology for PIN diodes and tuning varactors is given in Appendix A. This appendix addresses those stages in the production cycle that are influenced by contaminants and describes, in detail, the correlation of the device products to the manufacturing process.

1.3 SPECIFIC PROBLEM

There are uncertainties in processing semiconductor devices in reasonable yields consistently. Controls for times and temperature are known to be quite good. The most significant unknown is the variability of the chemical reagents and deionized water used in wafer fabrication. In addition, although ambient conditions are usually considered to be quite well-controlled with laminar flow, ultrafiltration and frequent particle counts, the chemical nature of airborne contamination is probably the next most significant unknown. The well-known cyclical history of the manufacture of certain microwave semiconductor devices bears these facts out. Frequently, certain devices go out of production; the company is said to have "lost the recipe" temporarily. Then, as mysteriously as the problem arose, its nature being such, the problem disappears; yields return to original levels and production once again returns. The cost to the Government in these situations is significant. Did the problem disappear because a particular lot of reagent material was used up, or replaced?

The problem could have been caused by variability within the manufacturer's specification of some critical contaminant in a reagent, as no quantitative tool is available to monitor on-line each batch for impurity levels and types.

The present project will form the basis for an automatic test and control system, which will include all the appropriate sensors to detect impurity levels in the chemical reagents and particulate matter which might be present in a microwave semiconductor process. This control system will have the capability of analyzing all the chemical inputs to the process, solid, liquid and gaseous. The functions of this detection and control system will be several: to provide warning of excessive contamination as early in the process as possible; to allow contaminated material to be discarded, rather than accrue further manufacturing costs; to be able to identify specifically the critical contaminants to microwave technology, and the

threshold levels necessary to precisely control the process; to provide lot traceability throughout the process so that final yields of end products can be correlated with known contamination levels and appropriate yield improvements can be made.

The benefit to the Government and to the microwave industry arising from this project is significant. The keystone of an overall process control and monitoring system is the analytical tool necessary to provide the answers as to what contaminants affect device yields, what are their allowable levels and what steps are to be taken to minimize their effects upon semiconductor yields.

The present project could readily be extended at some future date to include other sensors. Temperature, flow rates, real-time gas stream analysis, pressure, residual atmosphere under high vacuum are all areas which can be readily controlled and monitored by a computerized system. Historical information on the performance of a piece of equipment, comparison with present performance, and trend information are all readily available.

SECTION II

TECHNICAL APPROACH

2.1 GENERAL PLAN OF ATTACK

The solution to this problem must be based on, and must develop out of, an actual operating microwave semiconductor manufacturing facility. The data on which the solution is to be based can be meaningful only if it is derived from an on-line operating process and interpreted by individuals actively engaged with current technology and manufacturing practices. The solution must be tested at each stage of its evolvement against the realities of a microwave production line. Recognizing these requirements, PRD teamed with Microwave Associates, Inc., of Burlington, Massachusetts, which has been a major supplier of microwave semiconductor devices to the Army for many years and is currently manufacturing the high voltage PIN diode on which this study is based.

PRD and Microwave Associates have been designated as prime contractor and subcontractor, respectively. PRD has been charged with full responsiblity for the execution of the project and all liaison with the Procuring Agency. Microwave Associates, under the direction of PRD, will perform a major portion of the project work.

The instrumentation procured under this project will be installed in Microwave Associates in Burlington, Massachusetts, and operated by them. All chemical analyses will be made by Microwave Associates.

PRD will develop and exercise the analytical model and perform all statistical analyses. All computer requirements will be implemented on a UNIVAC 1108 computer resident at PRD, Syosset, New York. Data may be entered directly into the computer system via a remote terminal at Microwave Associates. All software programs will be written in FORTRAN IV.

Each member will contribute to the project as follows:

PRD will provide:

- Software development
- Computer facilities
- Systems Engineering
- Project Management

Microwave Associates will provide:

- Semiconductor Production Facility
- Microwave semiconductor technology

The team's approach to the solution of the problem is first to develop an analytical model of the semiconductor manufacturing process. The model will relate the concentration levels of each contaminant in each of the reagents to the levels in the semiconductor crystal and in turn to the product yield. These quantitative relationships will be expressed in terms of a set of parametric transfer ratios or coupling coefficients. The model will be exercised in parallel with the operation of the production line. Each intermediate step, as well as the final yield of the process, will be correlated with the corresponding step predicted by the model.

A system of item identification will be developed by which traceability can be maintained for each of the intermediate steps throughout the manufacturing process.

When correlation between the model and the process is achieved, to within reasonable tolerances, the model will be reduced to a linear-programming objective function suitable for optimization against any given set of constraints.

An analytical instrument will be procured to acquire the necessary data. The instrument will be capable of measuring contaminant levels to a few parts per billion. Using this instrument, the relevant transfer ratios will be determined.

An optimal set of contaminant threshold levels and monitoring points will be determined which will assure a specified maximum product yield at minimum unit cost.

Finally, the team will generate a specification for a system to monitor and optimize the microwave semiconductor manufacturing process under operating conditions.

2.2 ENGINEERING PROGRAM PLAN

Because of the long lead-time involved, the first task which had to be undertaken was the selection and procurement of an instrument capable of rapidly analyzing a substance for a large number of trace elements present in concentration levels of 10 to 100 parts per billion (ppb). After that was accomplished, arrangements would be made for its delivery, installation and acceptance and for the training of a staff of operators.

Simultaneous with the selection of the instrument would be the selection of a microwave semiconductor product line and a detailed definition of the manufacturing process involved.

Following that, work would start on the design and implementation of the analytic model and on the detailed design of the experiment. The latter would include the test and control runs to be made, the materials and instruments needed to make the runs and a plan for the acquisition of test data. With the completion of the test data acquisition plans, work could begin on the planning and implementation of the computer programs for managing and reducing these data. It was planned to complete all of the above by mid-January 1978 at which time the analytic instrument would have been installed and its operating personnel would have gained some experience in its use.

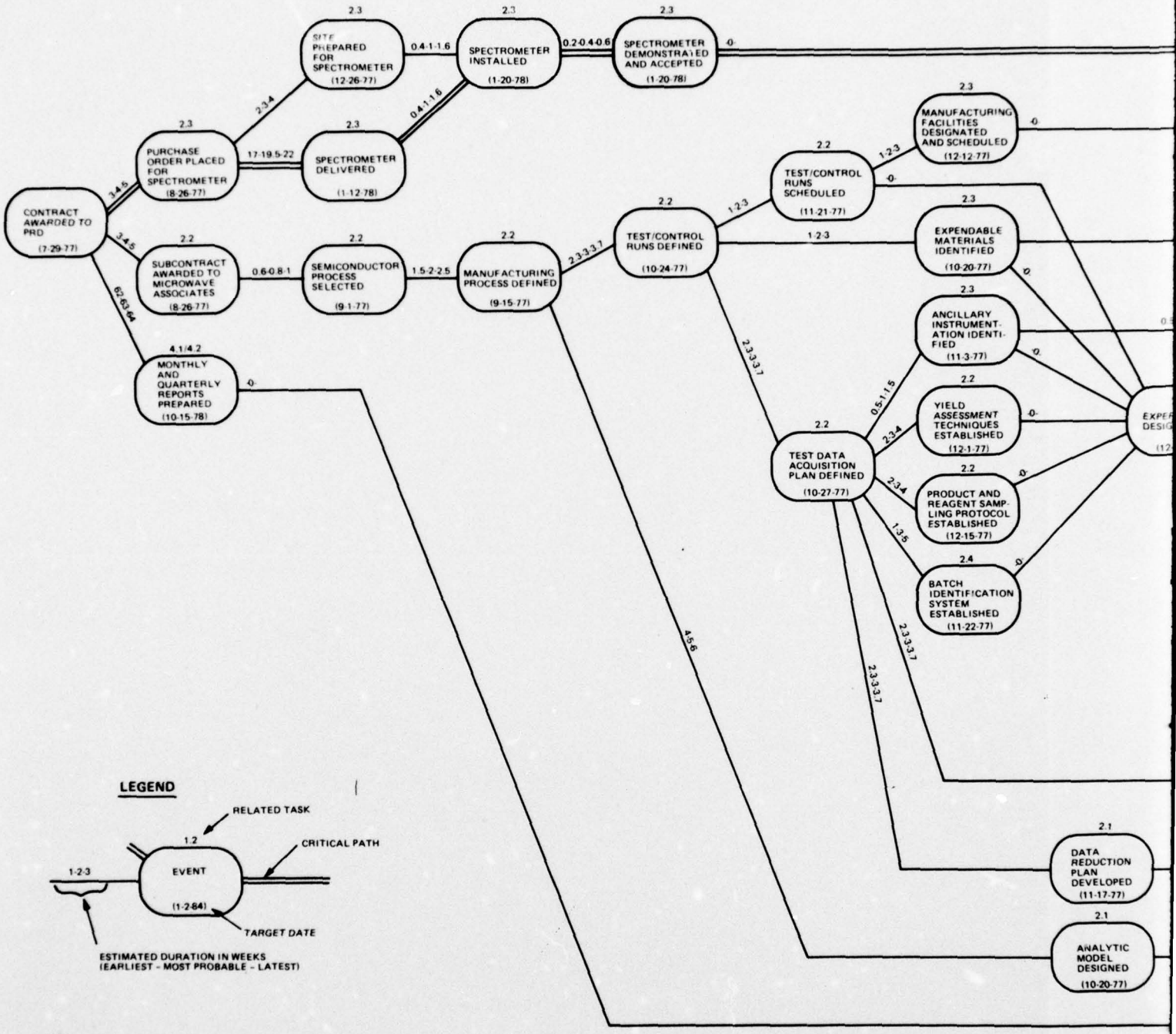
The period from mid-January through mid-March 1978 was scheduled for gathering experimental data on which to complete the analytic model, that is, determining its transfer ratios. Throughout that period, special experimental runs would be made using deliberately contaminated (doped) materials. By the end of

March, sufficient data would have been assembled to allow a preliminary verification of the model to be conducted. This would be accomplished using the model to predict the yield as one or more batches of wafers were processed. The remaining time through August 1978 would be devoted to refining the model and its optimization programs by gathering operating data from an otherwise normal production line process.

Once the form of the analytic model was verified, work would begin on the development of a system specification defining the integration of the new technique into a manufacturing process.

2.3 PERT SCHEDULE

Figure 2-1, Chemical Analysis System PERT, is a chart of the program indicating the general order in which the various tasks would be performed and the establishment of target dates for each.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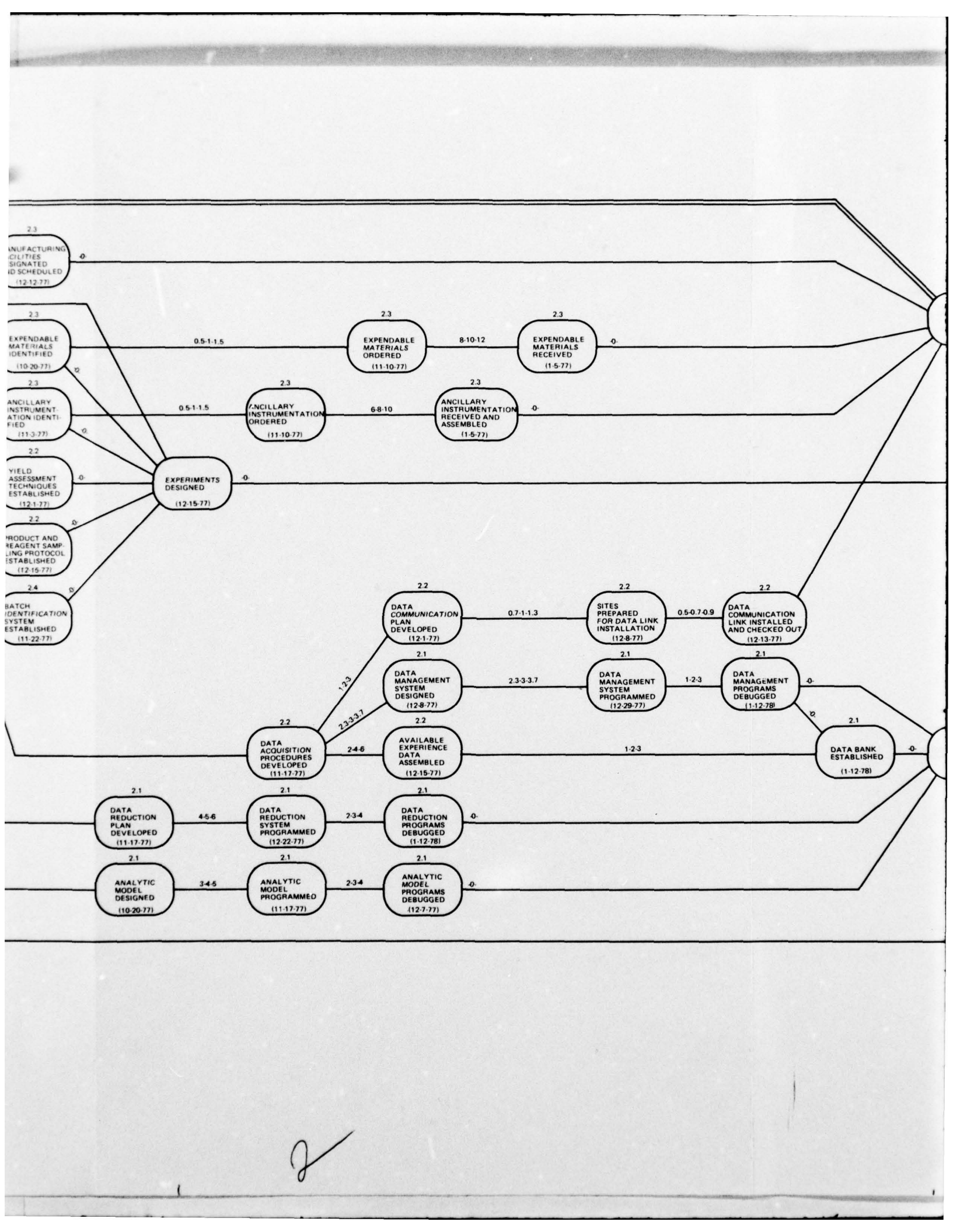
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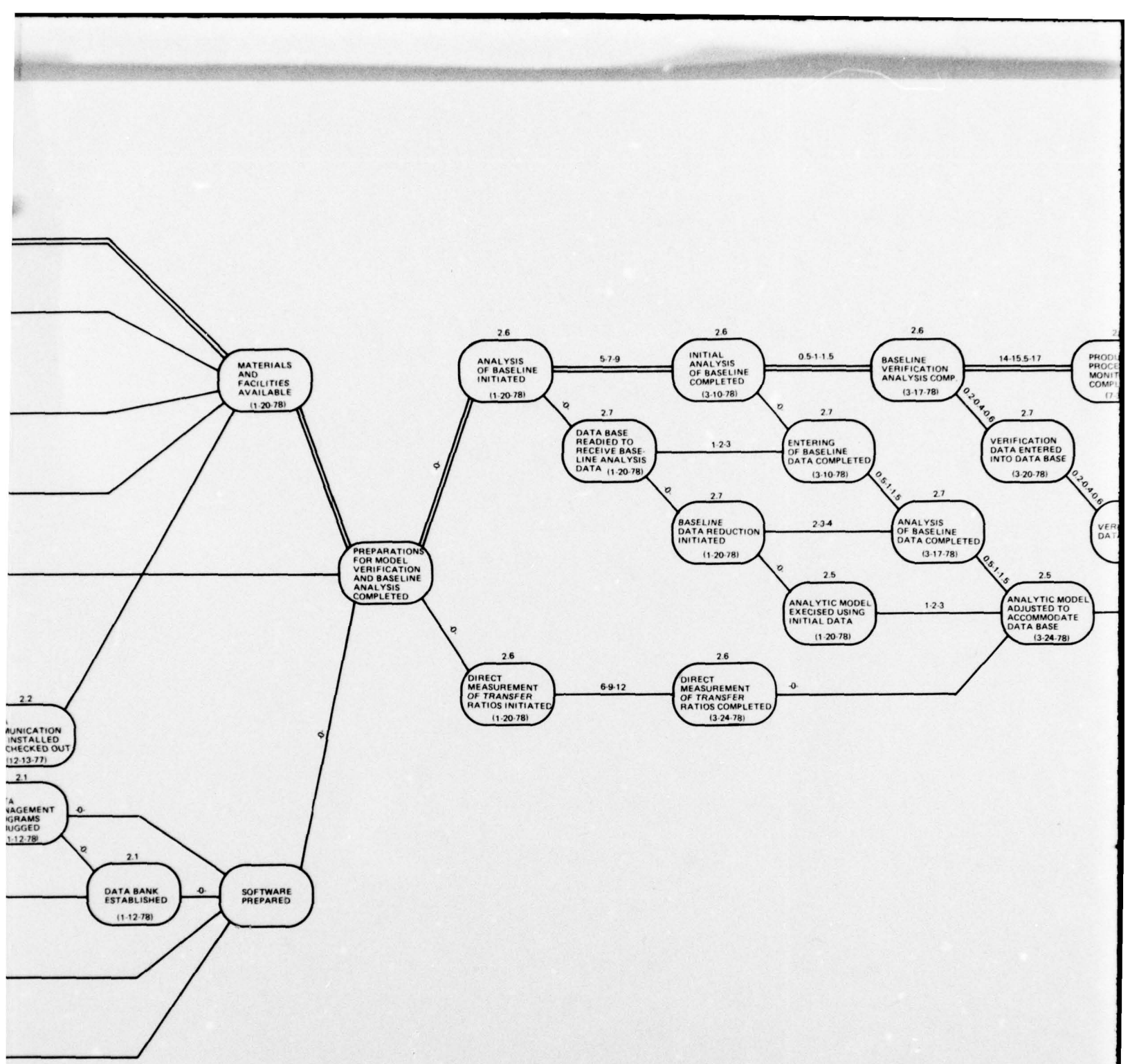
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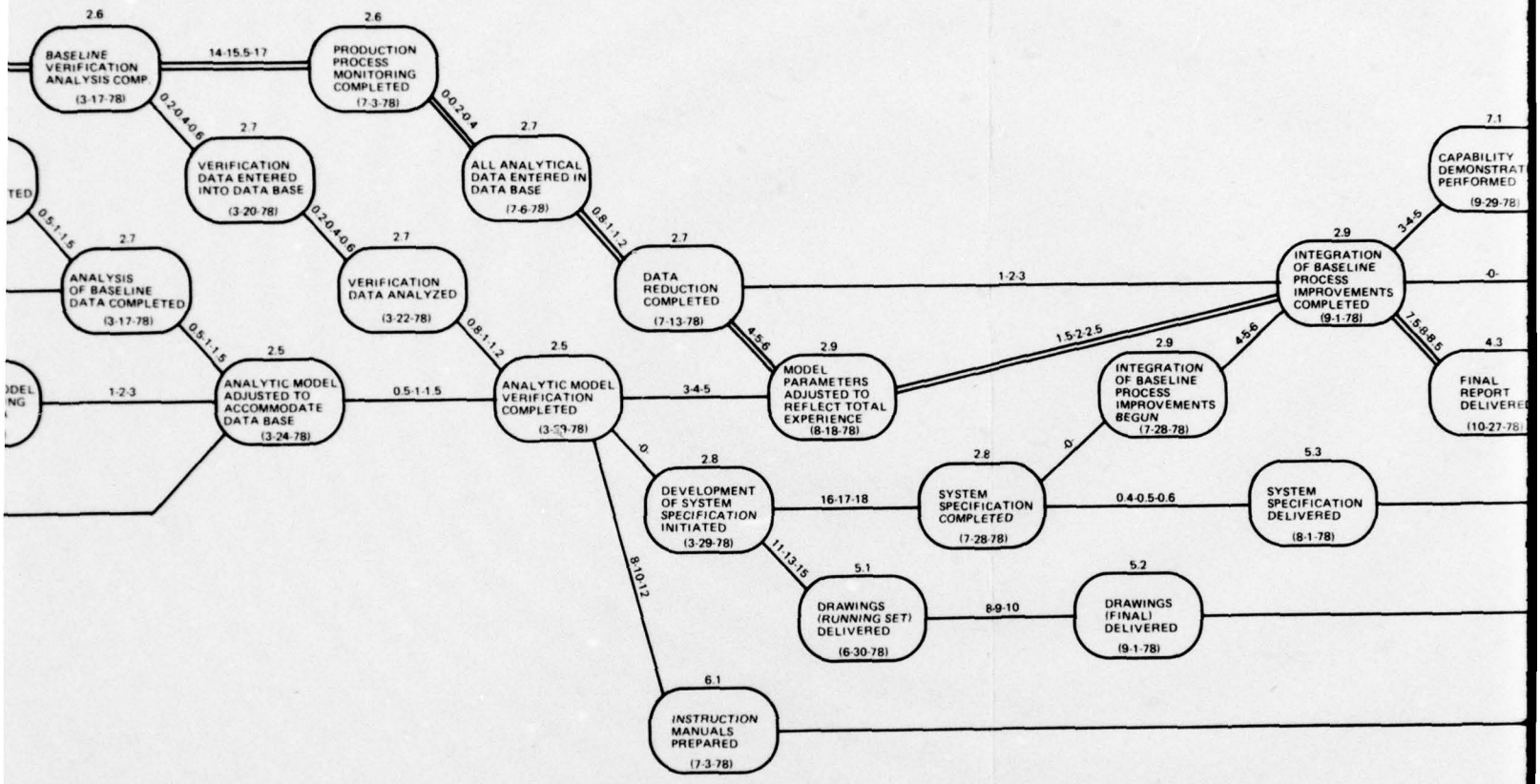

Figure 2-1. Chemical

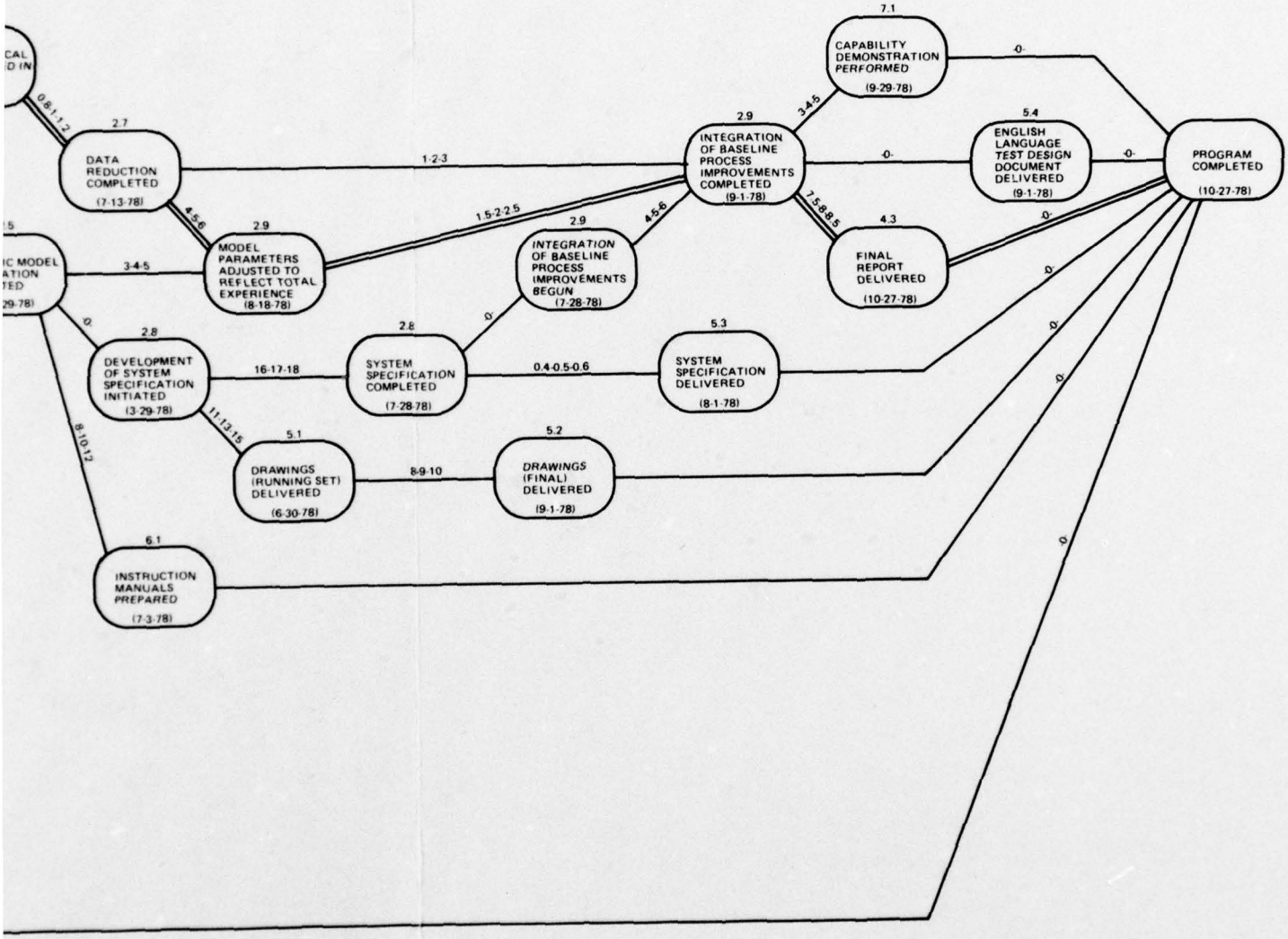

Figure 2-1. Chemical Analysis System PERT

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SECTION III

PROGRESS THROUGH OCTOBER 1977

3.1 INSTRUMENTATION

The primary analytical instrument selected for the project was a computer-controlled emission spectrometer with inductively coupled argon plasma atomization and excitation source (Plasma Atomcomp, Catalog Number 96-975 by Jarrell-Ash Division, Fisher Scientific Company). The instrument was capable of the simultaneous determination of 27 trace elements at the fractional microgram to nanogram level. The operation of the system was based on the observation of atomic emission spectra when a sample in the form of an aerosol, thermally generated vapor or powder was injected into an argon plasma. The plasma was formed by inductively heating a column of argon gas in a coil connected to a high-frequency generator operating in the 4 to 50 MHz range at a level of 2 to 5 kilowatts. The plasma attained a gas temperature in the 9,000-10,000° K (16,000 to 17,500°F) range. The resulting atomic emission spectra were then resolved in a classical direct reading spectrometer. Spectral isolation was achieved through 27 mechanical exit slits located precisely at the proper places along the focal plane. The light passing through each slit was sensed by a photo-multiplier tube. One photo-multiplier tube was used for each spectral line of interest. The electrical output of each tube was then multiplexed to a computer (Digital Equipment Corporation PDP-8). The computer was programmed to compute and print the concentration level of each element. The complete analysis of 27 elements was completed in approximately 30 seconds.

The rationale for the selection of the plasma spectrometer is set forth in Appendix B, Instrumentation Selection.

The instrument was scheduled to be delivered and installed in the microwave semiconductor facilities of Microwave Associates, Inc., Burlington, Massachusetts, on or about 20 January 1978.

3.2 PROCESS SELECTION AND DEFINITION

The process selected on which to base the technique was a 1,000-volt mesa PIN diode (e.g., JANTX-1N5710). The device was selected for the following reasons:

- The device had typically exhibited poor and erratic yields.
- It was a mechanically simple device which exhibited relatively few failures resulting from misalignments or improper assembly. It has only one welded connection.
- Microwave Associates had manufactured the device in large numbers and had amassed extensive experience in its manufacture.
- Microwave Associates had a production line in operation with well-defined operator procedures.
- The Army was currently using the device in large numbers.

Figure 3-1, Mesa PIN Diode Process, is a flow diagram of the manufacturing process which was selected.

3.3 ANALYTIC MODEL DESIGN

The analytic model of the microwave semiconductor device was designed and readied for programming. The design consisted of three systems of linear equations. The first was a system of non-homogeneous linear equations which related each process step and each measurement, whether a measurement be electrical, chemical or mechanical, to a function of the process yield and of the electrical descriptors (measurements) of the yield. The system addressed 50 process steps, 22 measurements and 35 chemical elements for a total of 1,722 coefficients.

A second system of equations reflected the structure of the ancillary or off-line operations, such as mixing several chemicals to form a bath. The system described 15 branch operations.

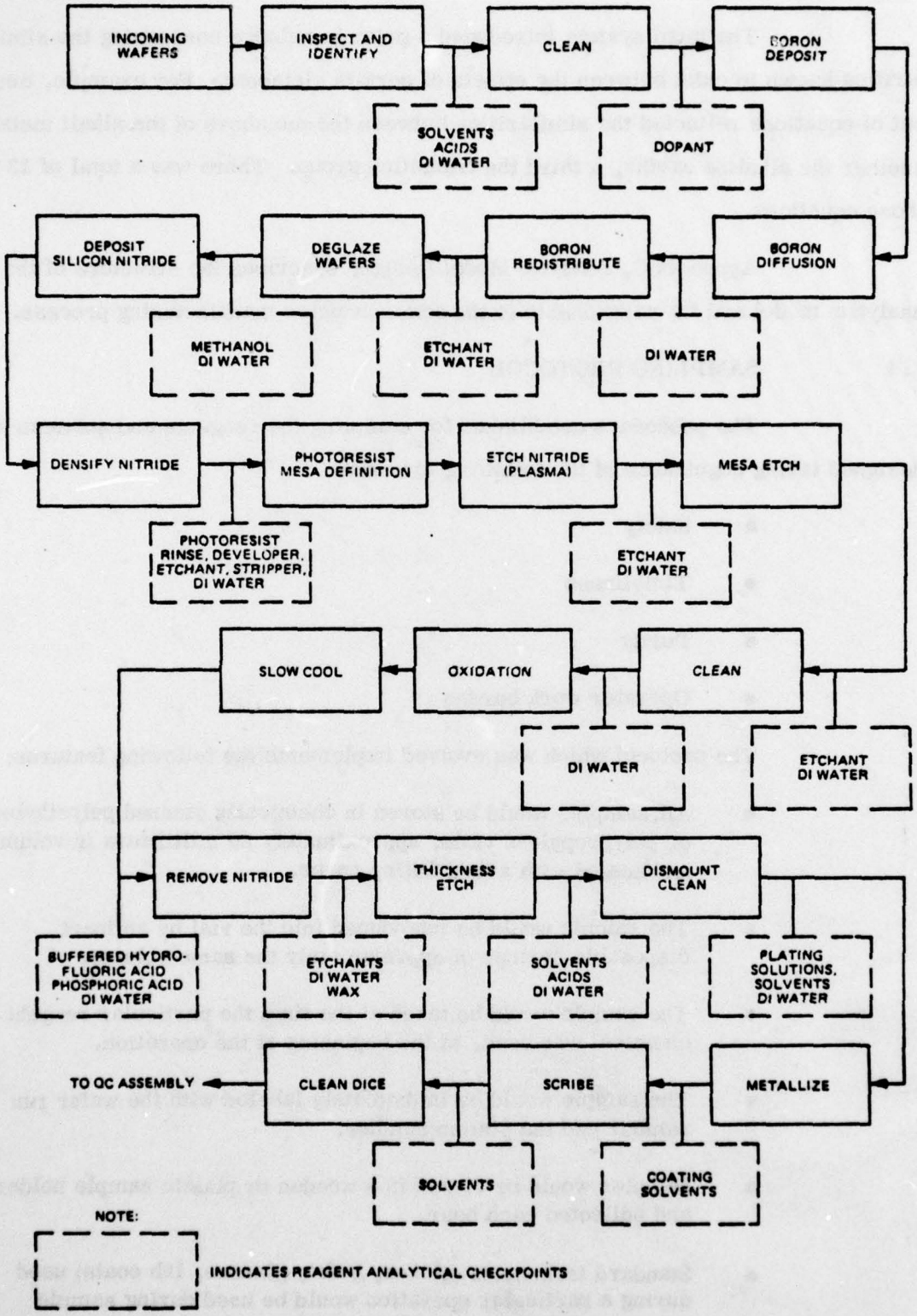

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Figure 3-1. Mesa PIN Diode Process

The third system introduced a prior knowledge concerning the similarities known to exist between the effects of certain elements. For example, one set of equations reflected the similarities between the members of the alkali metals, another the alkaline earths, a third the transition group. There was a total of 13 sets of those equations.

Appendix C, Analytic Model Design, describes the structure of the analytic model and its relationship to the semiconductor manufacturing process.

3.4 SAMPLING PROTOCOL

The procedure established for sampling the reagents and solvents was designed taking cognizance of the following criteria:

- Safety
- Timeliness
- Purity
- Operator work burden

The protocol which was evolved implements the following features:

- All samples would be stored in chemically cleaned polyethylene or polypropylene vials, approximately 20 milliliters in volume, and sealed with a tight fitting cover.
- The sample would be introduced into the vial by an inert disposable syringe of approximately the same volume.
- The sample would be taken at the time the particular reagent or chemical was used, at the beginning of the operation.
- The sample would be immediately labeled with the wafer run number and the station number.
- Samples would be stored in a wooden or plastic sample holder and collected each hour.
- Standard techniques (gloves, safety glasses, lab coats) used during a particular operation would be used during sample withdrawal.

- All samples will be taken at room temperature only.
- In as short a time as possible, each sample would be run on the spectrometer, and the data stored in the appropriate facility.

3.5 BATCH IDENTIFICATION

During the semiconductor processing phase of the program, both wafer identification and chemical or reagent lot identification will be maintained. Any interaction of a particular chemical with a particular wafer must be readily apparent. The following system was established for insuring traceability and providing unique identification:

- Wafers will be identified by scribing numbers, e.g., 1-10, on the "flat," legibly and small.
- Cross-reference between these numbers and the epitaxial run number will be made by transcribing both numbers on the back of an appropriate run sheet:

  for example: wafer #2 : epitaxial run R4781 Position #6

  #2 = R4781-6

  This provides traceability to the substrate and epitaxial growth.
- Wafers will then be grouped according to similar characteristics, and a "run number" will be assigned to each group. A group, then, might consist of 4-10 wafers.
- Chemicals and reagents will be identified as to their nature or type, and at which operation they are being used, by a "station" number. A particular type of chemical may be used at more than one station. In that event, it will be treated as an entirely "new" chemical each time it is used.

When a sample arrives at the spectrometer for analysis, its label will provide the following information:

- The identification of the wafer or wafers on which it was used
- The nature of the chemical or reagent
- The station at which it was used and at which the sample was withdrawn

For example:

Wafer Number	Chemical	Station Number
	GPA-1/TCL/14	
Epitaxial Run #GPA-1	Trichloroethylene	Rinsing Operation

3.6 YIELD ASSESSMENT

The primary objective of this MM&T project being "improvement of microwave semiconductor manufacturing process yields," it was imperative that a clear definition of yield be established at the outset. Many definitions of yield were considered: chips per kilogram of silicon boule, ratio of "good" chips to the total produced, yield relative to specific parametric threshold, yield to a particular distribution envelope of one or more parameters, etc. Sometimes yield can become ambiguous, if sufficient "fallout" specifications are imposed. Should a chip which does not meet one specification be considered for use in another less critical application? How should a wafer which was aborted in mid-process be accounted for?

For the purpose of this program, two somewhat different concepts of yield were adopted. The first, the one against which the success of the program will be measured, relates the number of chips produced which meet or exceed a given performance specification to the total labor expended in their production. Material costs were excluded because they represented only a small percentage of the unit costs and because they tend to fluctuate with the vagaries of the market. Including material costs would tend to moderate and obscure the effects of improved process monitoring. Yield (capitalized with a superscript bar) of the first type was defined as:

$$\overline{\text{Yield}} \equiv \bar{Y} \equiv \frac{\text{Total number of chips meeting or exceeding specification}}{\text{Labor units expended in producing chips}}$$

where:

$$\text{Labor Unit (LU)} \equiv \frac{\text{Man-hours expended in a particular process step}}{\text{Total number of wafers (chips) processed through the step}}$$

The concept of "Labor Unit," then, is directly related to the total number of wafers processed and can be related to a labor cost per wafer in dollars for that step. More importantly, the summation of labor units accounts for wafers which proceed part way through the process and are then aborted because the probability of their producing acceptable chips has fallen too low. Up to the time of being aborted they accumulate labor costs (labor units) and must be accounted for in the process yield as accrued costs, albeit they result in no product.

Using this definition, yield can be improved by several means:

- Increasing the number of acceptable chips produced for a given labor unit investment.
- Reducing the labor unit investment required to produce a given number of acceptable chips.
- Reducing the number of acceptable chips but with an offsetting proportionately larger reduction of labor units invested.

Let us consider for example, a hypothetical three-step process:

REFERENCE CASE

	Step 1	Step 2	Step 3	
Man-hours required for each step	1	2	3	
Number of wafers processed	10	10	10	
Labor units (man-hours per wafer)	0.1	0.2	0.4	
Total Labor Units Expended				0.7

Reference Case: Assume 10 wafers proceed through all three steps (no abortion) resulting in 50,000 acceptable chips

$$\overline{\text{Yield}} = \frac{50{,}000}{0.7} = 71{,}429 \text{ chips per LU}$$

Trial Case: Assume 10 wafers processed through the first step, 8 wafers (2 aborted) through the second step and 5 wafers (3 aborted) through the third step.

TRIAL CASE

	Step 1	Step 2	Step 3	
Man-hours required for each step	1	2	4	
Number of wafers processed	10	8	5	
Labor units (man-hours per wafer)	0.1	0.16	0.2	
Total Labor Units Expended				0.46

Assuming the trial case produced 70,000 acceptable chips:

$$\overline{\text{Yield}} = \frac{70,000}{0.46} = 152,174 \text{ chips per LU,}$$

an increase of 106 percent over the Reference Case.

Assuming the trial case produced 50,000 chips:

$$\overline{\text{Yield}} = \frac{50,000}{0.46} = 108,000 \text{ chips per LU,}$$

an increase of 52 percent over the Reference Case.

Assuming the trial case produced 20,000 chips:

$$\overline{\text{Yield}} = \frac{20,000}{0.46} = 43,478 \text{ chips per LU,}$$

a decrease of 39 percent over the Reference Case.

Finally, assuming equivalent $\overline{\text{Yields}}$ for both cases, i.e., 71,429 chips per LU, the Reference Case would produce 50,000 chips while the Trial Case would produce 32,857 chips for 0.24 fewer labor units. The Trial Case would produce 54 percent fewer chips for 66 percent less money.

By defining $\overline{\text{Yield}}$ in this manner we will be able to account for the impact of aborting wafers early in the process when the analytic model predicts the probability that the wafer, if carried through to completion, would produce an insufficient number of acceptable chips.

To this point we have addressed only an average $\overline{\text{Yield}}$ (capitalized with a superscript bar), that is, a yield associated with a plurality of wafers. When yield is associated with the number of acceptable chips, whether actual or projected, derived from a single wafer or group of identical wafers, as in the case of the

analytical model, the term must take on a somewhat different meaning. In this case the term can apply only to wafers which are assumed to have completed the entire process and accrued a common labor unit level. In this case, yield will be simply the non-dimensional ratio of "acceptable" chips to the total population of chips and will be designated by omitting the superscript bar.

How should yield be measured? The objective of the present project is to establish the correlation between impurities in the materials and the electrical properties of the product. This being the case, factors which affect the yield but are not attributable to contaminants, such as edge effects, non-uniform layers, and tapering of the wafer are irrelevant and should be discounted, insofar as practical. Therefore, data will be gathered from only the most uniform portion of the wafer. In a 2-inch diameter wafer, a 1-1/4-inch diameter circle centered in the wafer will be designated as the "test area." Assuming a 2-inch diameter wafer and chips that are 0.035 inch square, a total chip population of 2,500 units is available. In a 1-1/4-inch diameter circle, there would be approximately 1,000 chips, or 40 percent of the total population, available on which to base yield measurements.

SECTION IV
CONCLUSIONS

4.1 DATA ACQUIRED

The first quarter was devoted entirely to planning the experiment, acquiring the analytical instrumentation, and preparing computer programs. Not until the early part of the third quarter will experimental data be developed or any conclusions drawn.

4.2 OVERALL PROGRESS

All major milestones and target dates were met through 31 October 1977, the end of the first quarter. (See figure 2-1, Chemical Analysis PERT Chart.)

SECTION V

PROGRAM FOR NEXT INTERVAL

5.1 SECOND QUARTER TASKS

a. Instrumentation and Training. The spectrometer is scheduled for delivery and installation during the last week of November 1977. The installation will be made at the facilities of Microwave Associates, Inc., Burlington, Massachusetts, where a separate laboratory room has been prepared. The laboratory has been equipped with the necessary utilities including electrical power, cooling water, safety ventilation and telephone/data lines as well as supplies of argon gas and deionized water.

b. Installation and Calibration. These will require about 3 weeks to complete. This will be a somewhat longer period than originally anticipated, but, because the instrument will be delivered approximately 4 weeks earlier than scheduled, the overall project will not be adversely affected.

Training in the use of the spectrometer, which was originally scheduled for the third week in November, was rescheduled because of a conflict at Jarrell-Ash Division and will be carried out during the third week of January 1978.

The instrument will be installed and calibrated and operating personnel trained by the third week of January 1978, at which time data collection will begin. These data will be gathered and temporarily stored on a floppy disk system (Digital Equipment Corporation RX11 Floppy Disk System) and subsequently transmitted to PRD, Syosset, New York, on a daily basis via telephone data line.

c. Design of the Experiments. The design of the experiments which are to be conducted and the definition and scheduling of the test sample runs will be completed during the second quarter in time for their initial implementation by the time the spectrometer is installed and calibrated.

d. Data Reduction Program. Because there are over 1,700 factors to be evaluated in the analytic model, the major effort during the second quarter will be devoted to a search for techniques of data reduction which will minimize the amount of experimentation required. This task will have to be worked in concert with the design of the experiments.

The techniques of optimization have been well-defined. During the second quarter these will be programmed and debugged. No problems are anticipated in this area and progress should be orderly. They will be completed and ready to run by the end of the second quarter.

e. Data Management Programs. Like the techniques of optimization, the programs for managing the data bank are well understood and preparation of the computer programs will be routine. These programs will be debugged and ready by the end of the second quarter.

f. Analytic Model Programming. The analytic model design was completed during the first quarter and will be programmed and debugged during the second quarter.

5.2 MAJOR TECHNICAL PROBLEM AREAS

The major technical problem which will be addressed during the second quarter will be that of finding techniques which will minimize the amount of experimentation required in the evaluation of the over 1,700 factors of the analytic model. Our initial approach will be twofold. First, we will attempt to divide the essentially serial process into smaller segments such that a single batch of wafers going through the complete process will provide information on several subsets at one time. This will permit solving two or more subsets of equations rather than one set of more than 1,700 simultaneous equations.

The second approach will be to make use of the data that exists concerning the relative behavioral characteristics of the elements to effectively reduce the number of elements to a smaller number of elemental groups. For example,

if we can group all of the alkali metals into a single composite it would reduce the task by approximately 10 percent. If we could combine the two alkaline earths, magnesium and calcium, the task would be reduced by another 3 percent.

SECTION VI

PUBLICATIONS AND REPORTS

(There were no publications, conferences or talks made during the period covered by this report on or associated with the work performed under Contract No. DAAB07-77-C-0561).

SECTION VII

IDENTIFICATION OF PERSONNEL

7.1 PERSONNEL WORKING ON PROGRAM

Personnel working on the program and the hours worked through the period of performance of this report are:

Roy W. Spacie, PRD Electronics	408 hours
Dr. George P. Allendorf, Microwave Associates	164 hours
Albion Weeks, Microwave Associates	120 hours

7.2 PERSONNEL BACKGROUND

Roy Spacie. In his current assignment Mr. Spacie is responsible for coordinating all technical activities toward the successful fruition of the Chemical Analysis Program.

Previous experience included responsibility for the development and direction of radar system activities in the field of foreign technology. He was responsible for the organization and direction of advanced studies and developments in the field of synthetic aperture high-resolution radar systems. He has also served on special assignments to the Ground Systems Department in charge of technical liaison to subcontractors engaged in large scale computer software development programs and served as a consultant in the Advanced Projects Department in charge of new business development activities for electronic ground systems including computer applications. His major contributions were in the areas of signal processing, vibration analysis, acoustic emission and automatic pattern recognition.

Mr. Spacie had served as Assistant Chief for Advanced Design and as Assistant Director of Research.

Mr. Spacie was graduated from Northern Illinois State University with a BS in Physics in 1936 and has successfully completed graduate courses in Mathematics and Electrical Engineering at the University of Illinois, Princeton University and Massachusetts Institute of Technology.

Dr. George Allendorf. In his current assignment, Dr. Allendorf is responsible for fiscal, technical and production performance of the silicon process group involved in the chip manufacture of PIN, multiplier varactors, Schottky, and beam lead diodes.

Previous experience included technical participation as a project team member and subsequently as operational manager for Microwave Associates' original development effort in low-noise UHF and microwave transistors. He developed a family of low-noise UHF transistors and wrote manufacturing specifications for this family. He also developed the original shallow-diffusion schedules and the process scheme for low-noise microwave transistors (f_T = 4-4.5 GHz).

Dr. Allendorf previously specialized in metallization in the development and production of high power, glass passivated PIN diodes used in the phased array MSR. He developed process sequences and developed the particular metallization scheme (patent applied for) which was compatible with the very sensitive glass passivation, which led to high assembly yields from a bonding and R_s point of view, and had extremely high reliability from a failure point of view.

Dr. Allendorf was graduated from Worcester Polytechnic Institute, Worcester, Massachusetts, with a PhD in Physical Chemistry in 1970. He also possesses an MS in Physical Organic Chemistry (1965) from Holy Cross College Worcester, Massachusetts, and a BS in Chemistry (1961) from Boston College, Massachusetts.

SECTION VIII

ADDITIONAL REPORT INFORMATION

8.1 SPECTROMETER

The work of this project required the simultaneous determination of trace elements at microgram or nanogram levels. For this purpose, a computer-controlled emission spectrometer was selected which employed an inductively coupled argon plasma excitation source. The rationale for the selection is set forth in Appendix B. The operation of the spectrometer is based on the observation of atomic emission spectra when samples of the analyte in the form of an aerosol, thermally generated vapor, or powder were injected into the plasma of a flame source. The plasma served both to atomize the analyte and excite it to optical emission.

The instrument selected was a Jarrell-Ash Atomcomp which comprises five principal components: a spectrometer, a plasma torch and aspirator, a radio frequency power source, a control computer, and a hard-copy printer/terminal. The spectrometer is a classical multichannel direct reading optical (ultra-violet) emission spectrometer of the type shown schematically in Figure 8-1, Schematic of Direct Reading Spectrometer. Optical spectra emitted in the plasma torch were focused on an entrance slit by means of a lens system. The light admitted by the entrance slit was made to fall upon the closely ruled surface of a diffraction grating, from which it was reflected and dispersed into its color (frequency) spectrum. Spectral isolation was achieved through mechanical exit slits located precisely at the proper place along the focal plane (Rowland circle). In this way spectral isolation was achieved for 27 elements simultaneously.

Mounted immediately behind each slit, outside the Rowland circle, is a plane mirror and a photo-multiplier tube. Immediately associated with each photo-multiplier tube is a printed circuit card containing an electronic amplifier

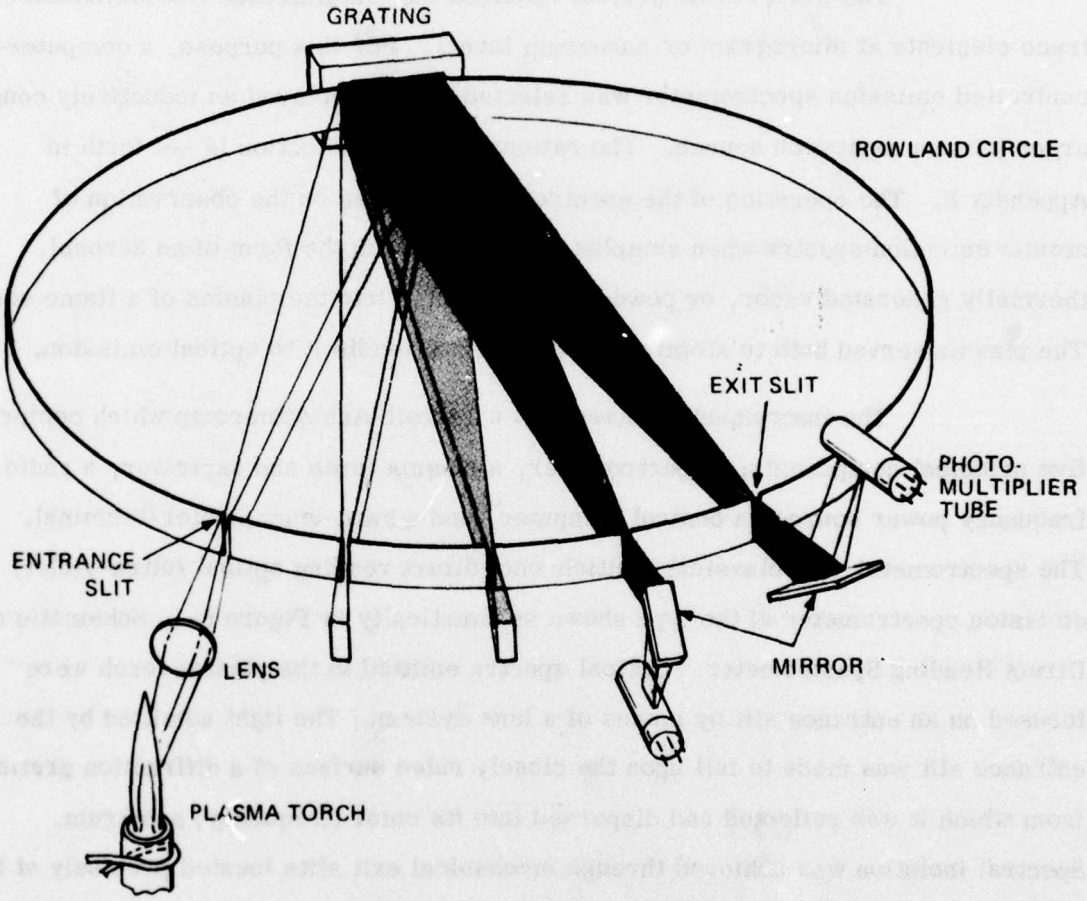

Figure 8-1. Schematic of a Direct Reading Spectrometer

and gated integrating circuit. The photo-multiplier tube sensed the light falling upon it and generated an electric current proportional to the intensity of the light. The associated electronic gating (switching) circuit allowed the current from the photo-multiplier tube to flow into an integrating capacitor for a precisely controlled time interval, thus developing an electric voltage across the capacitor proportional to the light intensity.

The spectrometer was controlled by a mini-computer (Digital Equipment Corporation Model PDP-8/E). The computer had 8,192 twelve-bit words of core storage with a 1.2-microsecond memory cycle time and 130,000 words of mass storage in the form of a dual-floppy disk (Digital Equipment Corporation Model RX11).

In operation, the control computer interrogated (sampled) each photo-multiplier tube's storage capacitor in rapid succession. It measured the stored voltage on each capacitor and discharged each in turn, returning it to a zero reference voltage level. From the measured voltage, the computer calculated the concentration of each of 27 elements. All 27 concentrations were provided in less than 1 minute.

The source of the spectra was a unique plasma torch which served to atomize and excite the analyte to incandescence. The operation of the plasma torch was based on the fact that plasma, being a gas in which a significant fraction of the atoms or molecules are ionized and capable of conducting an electric current, interacts with magnetic fields. Time-varying magnetic fields inductively couple to a plasma in a manner analogous to the inductive heating of metals.

Referring to Figure 8-2, A Simplified Plan of a Plasma Generator, a quartz tube approximately 2.5 centimeters in diameter was placed inside an induction coil connected to a high-frequency generator operating typically in the 4 to 50 MHz range at a generator output level of 2 to 5 kilowatts. A flow (5 liters per minute) of argon gas was directed through the quartz tube. Since argon is a nonconductor of electric current at room temperature, nothing happened, that is, until free electrons were released within the coil space. This was achieved by means of an electrical discharge or spark from a Tesla coil. The high-frequency current flowing in the induction coil generated an oscillating magnetic field whose lines of force were axially oriented inside the quartz tube and followed in nearly elliptical closed paths

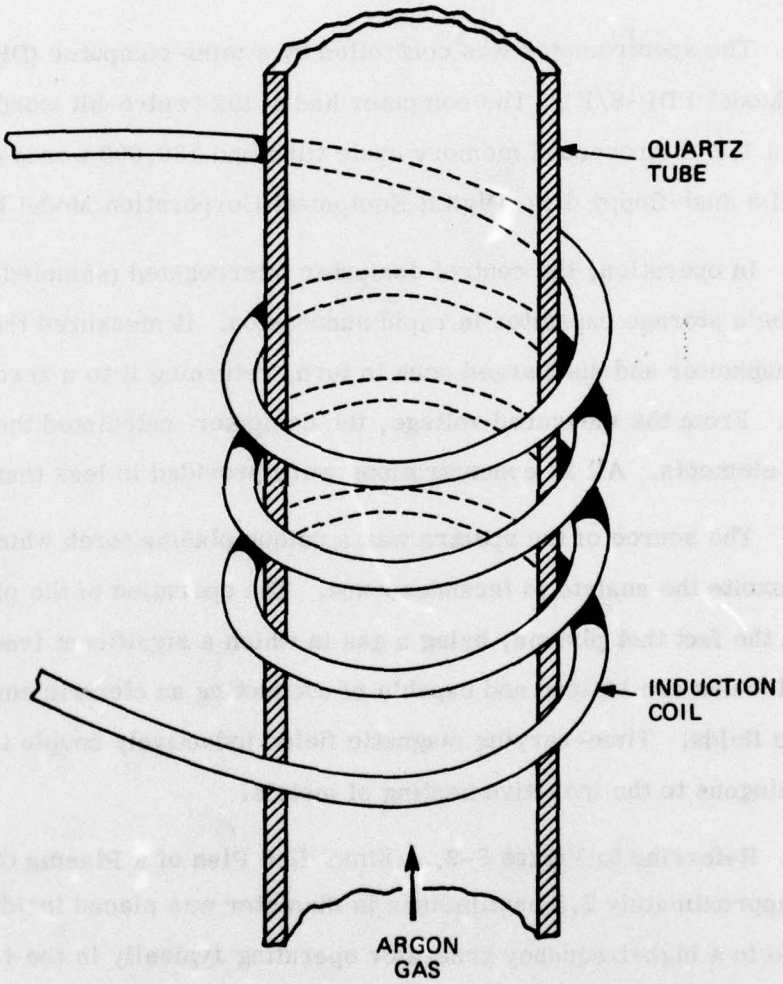

Figure 8-2. A Simplified Plan of a Plasma Generator

outside the coil as shown in Figure 8-3. The induced axial magnetic field within the quartz tube reacted with the electrons released by the Tesla coil discharge, causing them to flow in an annular path inside the quartz tube space. This electron flow, an eddy current, was analogous in behavior to the current flow in a short-circuited secondary of a transformer. The electron flow, meeting ohmic resistance, produced joule heating which, in turn, produced additional ionization, resulting in the formation of a sustained plasma.

The plasma formed in this manner attained a gas temperature in the 9,000-10,000° K range in the regions of maximum eddy current flow. Thermal isolation of the plasma to prevent overheating of the quartz tube was achieved by creating a vortex of relatively cool argon between the plasma and the quartz. This was accomplished by introducing a tangential flow (5 liters per minute) of argon gas which created a Reed's vortex to contain and stabilize the plasma.

The analyte was injected axially into the plasma by a second, much smaller, stream of argon, as in Figure 8-4. The sample stream of argon carried the analyte either as an aerosol, a powder or a thermally generated vapor.

The plasma torch resembled the conical flame of a Bunsen burner, the plasma had the overall appearance of a very intense, brilliant white, non-transparent core and a flame-like conical tip. The tip was bright but nearly transparent. It was this upper portion of the plasma which assumed typical flame colors when analytes were injected into the plasma.

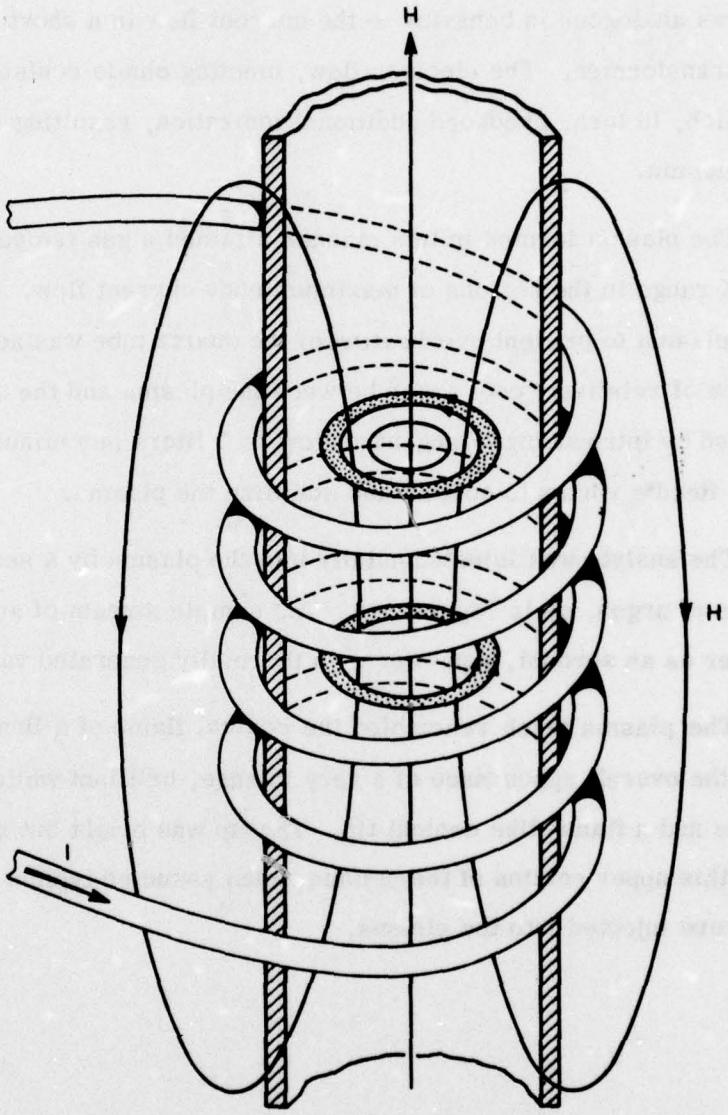

Figure 8-3. Axial Magnetic Field and Eddy Current Region in a Plasma Generator

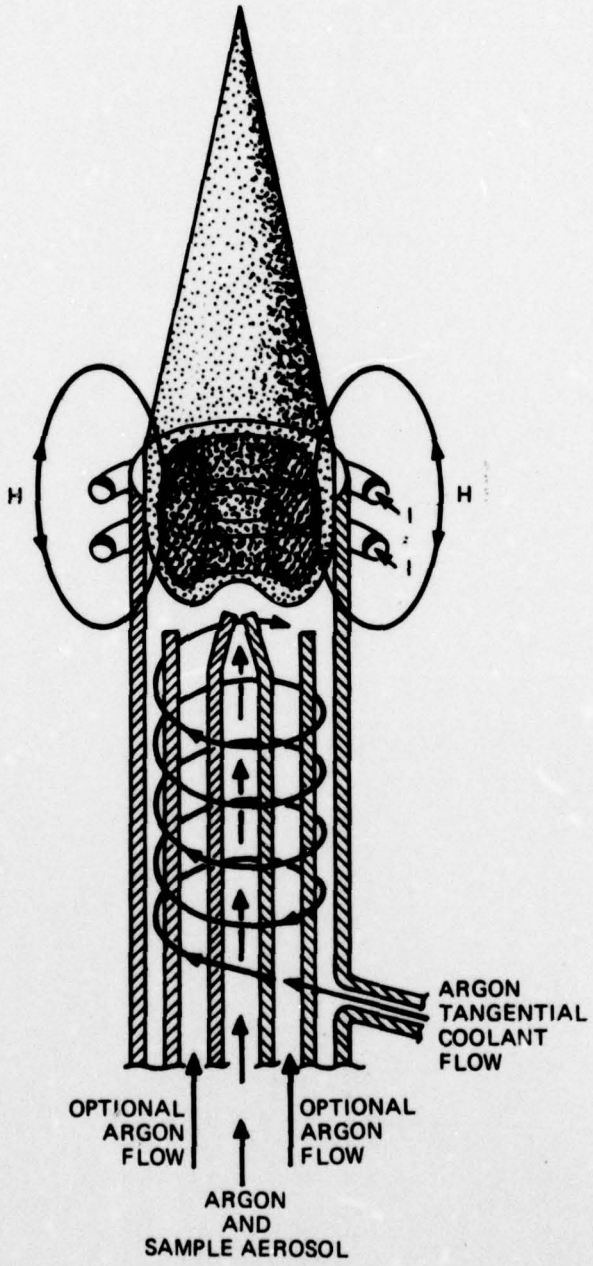

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Figure 8-4. Plasma Torch

APPENDIX A

A.1 MICROWAVE SEMICONDUCTOR DEVICE TECHNOLOGY

A.1.1 Introduction

Semiconductor devices manufactured for use at microwave frequencies generally originate from one of three basic semiconductor materials: silicon, germanium, or the compound semiconductor, gallium arsenide. Each step of the manufacturing process, from the formation of the original crystal ingot to the final encapsulation of the device chip, affects the yield and subsequent cost of the device. Contamination is constantly a threat, entering from any of the multitude of chemical operations, physical operations, handling, ambient changes, and all other combinations which we refer to as a process sequence. It is imperative, therefore, to manufacture the device in the cleanest, most controlled, most reproducible type of environment possible.

Microwave devices most often are designed with voltage breakdown, capacitance, series resistance (including minority carrier lifetime), the capacitance-voltage slope and leakage currents as the primary considerations. In order to provide the correct combinations of the above parameters, silicon of appropriate conductivity types, resistivities and thicknesses are necessary. The usual method to accommodate this need is to epitaxially deposit silicon of desired conductivity, resistivity and thickness onto the appropriate polished silicon substrates. This procedure results from the thinness of the layer which must be achieved (e.g., 2-6 microns) and the resistivity range which can be spanned (e.g., 0.01 to > 500 ohm•cm) while retaining the crystalline perfection found in the substrate. The substrate furnishes the required mechanical strength while minimizing the series resistance of the final structure. Junction formation is accomplished by Schottky barrier metallization or by p-n junction formation by diffusion or ion implantation.

The operational function of a device, whether it be a PIN diode, a varactor, or a microwave transistor, depends on controlling impurities of known type (both donors and acceptors) as to their concentration and position in the host semiconductor lattice. Concentrations of these "controlled" impurities are as low as one part per billion, and the depths to which they are diffused, implanted, or otherwise introduced are controlled often to a fraction of a micron. Should the level of noncontrolled impurities in or on the semiconductor reach some critical value, especially before a high temperature process occurs, device failure can be expected. Often, the concentration of impurities necessary to degrade device performance is only a fraction of the "controlled" amount of impurity dopant necessary to provide device performance.

A.1.1.1 Basic Material - The beginning of life for a silicon microwave device is the preparation of bulk silicon which occurs in a quartz crucible at temperatures exceeding 1,400°C in an atmosphere of ultrapure argon. Depending on the resistivity desired, controlled amounts of dopant (usually highly purified elemental boron, arsenic, or antimony) are added to the melt, and a crystal seed of the appropriate orientation is suspended at the interface. Slowly, the crystal is "pulled" from the melt; the structure, defect content, and diameter are controlled by the rate of pull. When the desired length is obtained, the ingot is removed.

If very high resistivity (e.g., 1,000-10,000 ohm·cm) silicon were desired, a process of purification called zone refining would be performed on the ingot. During this process, a molten zone, in which the dissolved impurities are preferentially segregated, is slowly moved down the length of the ingot and crystallized at the end, where, after repeated passes, it is cut off and discarded.

Mechanical and chemical operations then follow, as the ingot is surface-ground, etched chemically to remove mechanical damage, cut into slices with a diamond saw, etched chemically to remove saw damage, and finally chemically and mechanically polished. The polished wafers are evaluated for resistivity and then put into stock to await subsequent epitaxy.

Epitaxial growth of silicon is a chemical vapor deposition process usually carried out at temperatures in excess of 900°C, onto silicon or sapphire (Al_2O_3) substrate. During this process, bulk silicon wafers, doped to a very low resistivity (0.002-0.01 ohm•cm) either with arsenic, antimony or phosphorous for n^+ type, and boron for p^+ type, are placed flat on a graphite or silicon carbide coated susceptor. The side of the wafer on which epitaxial growth is to occur has been highly polished chemically and mechanically. By means of RF induced heating, the susceptor and silicon wafer are brought to an elevated temperature, where the slices are given a surface cleaning by means of the etching reaction:

$$Si_{(solid)} + 4\ HCl_{(gas)} \xrightarrow[H_2]{\Delta} Si\ Cl_{4\ (gas)} + 2H2_{(gas)}$$

After etching the surface slightly (perhaps 0.5 mil of silicon is removed), the chemical vapor deposition is initiated. For example, silane is decomposed in the presence of hydrogen by the following:

$$Si\ H4 \xrightarrow{\Delta} Si_{(solid)} + 2H2_{(gas)}$$

At elevated temperatures, the silicon atoms have enough thermal energy on the surface to be able to seek out crystalline sites, where they condense, thus continuing the crystalline structure, and hence the name, epitaxial growth.

After epitaxial growth, thickness of the epitaxial layer is generally measured by an infrared reflectance technique, which is analogous to the Bragg technique of X-ray analysis for crystal structure. Thus, the thickness of the layer can be determined by the spacing of the interference fringes in the infrared reflectance spectrum. In addition to this nondestructive test, angle lapping or cross sectioning and staining can be used to observe and measure the depth of the metallurgical interface; however, this latter is a destructive technique and is only performed on a sample basis.

The resistivity of the epitaxial layer can be determined by four-point probe measurement. The profile of the layer, and abruptness or gradedness of the interface can be determined analytically by either a differential capacitance technique

or the Copeland technique, named after its inventor. In either technique, the actual profile, i.e., impurity atoms as a function of layer thickness, is obtained. These data are usually presented in graphic form so that very quickly one can conclude much about the starting material.

At this point, the silicon wafers (referred to as n/n^+ or p/p^+) are put into inventory, with their identifying characteristics (resistivity, thickness of layer, resistivity and dopant type in the substrate and epitaxial run number).

A.1.1.2 Device Processing

A.1.1.2.1 General Environment

Before considering a more formal process flow chart for the manufacture of silicon microwave devices, let us consider the manner and environment wherein silicon wafers are processed. Silicon wafers are typically processed in batches to minimize wafer handling and breakage; these batches are transported in containers which have been dutifully cleaned and are handled either by tweezers or vacuum pickups which have been thoroughly degreased. Finger or glove contact is never allowed and individual handling is minimized. Storage of wafers at selected points in the process is normally at points where the silicon is protected with a silicon dioxide layer, and the wafers are in closed containers, usually in an inert gas atmosphere.

The typical fabrication process now becomes more specific for the actual final device parameters needed. Wafers are drawn from inventory in a lot and, accompanied by a lot traveler indicating the process steps and control points, are started through the process. Generally, in the mesa or planar process, wafers are subjected to high temperature thermal oxidation, chemical cleaning, high temperature boron or phosphorous diffusion, photolithography, etching, solvent cleaning, and vacuum or wet metallization. The sequence depends on whether a mesa device, or the more recent planar device, is desired.

Process fabrication facilities are typically laminar flow, Class 100 (or at least Class 100 in the process areas), with particle counts monitored on a scheduled basis. Class 100 indicates no more than 100 particles (whose maximum

size is 10^{-4} cm (1 micron) per cubic foot of air. Temperature and humidity control are necessary and must be constant from day to day.

A.1.1.2.2 Types of Devices

Microwave semiconductor devices may be constructed in either a planar or a mesa configuration. Representative examples of these two types of devices utilized for PIN diodes are shown in Figure A-1 and a typical mesa tuning varactor structure is shown in Figure A-2.

A generalized process flow chart for the planar process is shown in Table A-1 and the process subsequent to epitaxial growth and prior to encapsulation is shown schematically in Figure A-3.

A generalized process flow chart for the mesa process is shown in Table A-2 and this process is shown schematically in Figure A-4.

A.1.1.2.3 General Processes

The major processes involved in these devices are thermal oxidation, photolithography, boron diffusion mesa etching, contact metallization, dicing and encapsulation. Implicit in these processes are wafer cleaning procedures at each step of the processing.

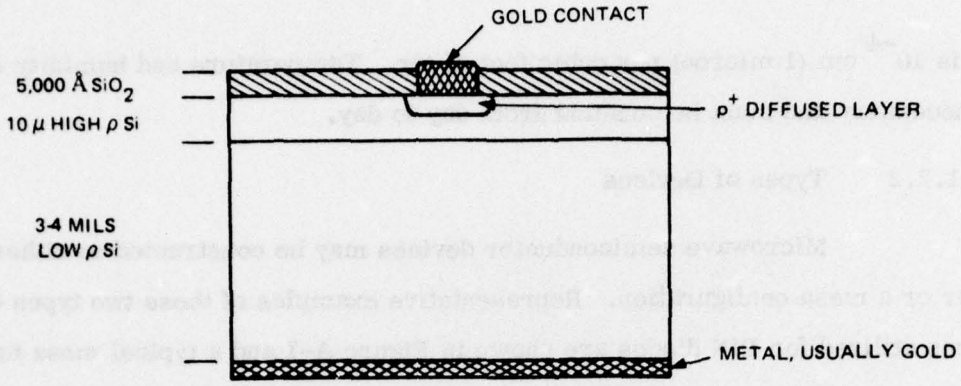
Thermal oxidation is performed on silicon for several reasons, depending on the point in the process. One function of the grown silicon dioxide layer is to mask areas of the silicon from the dopant atoms to be introduced later. Thus, in the planar process, 2,000-6,000 Å of SiO_2 is grown thermally by the following reactions:

$$Si_{(solid)} + O_{2\,(gas)} \longrightarrow SiO_{2\,(solid)}$$

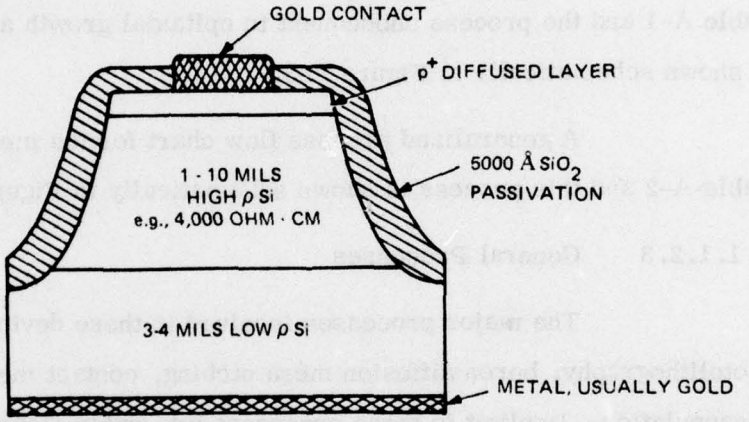
or

$$Si_{(solid)} + 2H_2O_{(gas)} \longrightarrow SiO_{2\,(solid)} + 2H_{2\,(gas)}$$

depending on whether the oxidation is performed in a wet or dry O_2 atmosphere. Reasonable oxidation rates for silicon occur in the temperature range of 900°C to 1,200°C. An equally or more important function of an SiO_2 layer is to passivate the



a. Planar PIN Chip



b. Mesa PIN Chip

Figure A-1. Representative Examples of Planar and Mesa Devices

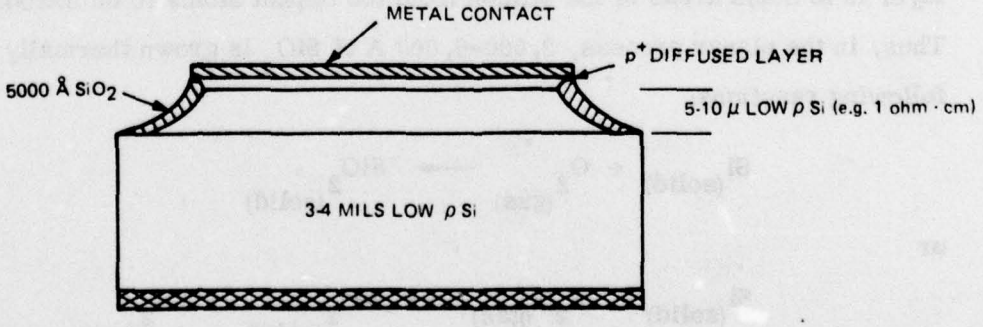


Figure A-2. Mesa Tuning Varactor Chip

TABLE A-1. GENERALIZED PROCESS FLOW CHART - PLANAR DEVICE

Substrate: Low resistivity antimony or arsenic doped polished silicon

1. Epitaxial Growth
2. Clean
3. Thermal Oxidation
4. Photolithography
5. Boron Deposit and Diffusion
6. Thermal Oxidation
7. Photolithography - Contact
8. Thickness Adjustment
9. Contact Metallization - Both Sides
10. Dicing
11. Die Mount
12. Wire Bond
13. Cap (or Seal)
14. Test and Screen
15. Ship, Inventory

TABLE A-2. GENERALIZED PROCESS FLOW CHART - MESA DEVICE

SUBSTRATES

1. Epitaxial Growth
2. Clean
3. Thermal Oxidation
4. Mount and Strip Oxide, Epi Side
5. Boron Deposit and Diffusion
6. Thermal Oxidation
7. Photolithography
8. Mesa Etching
9. Mesa Passivation
10. Photolithography
11. Thickness Adjustment
12. Contact Metallization, Both Sides
13. Dicing
14. Die Mount
15. Wire Bond
16. Capping (or Sealing)
17. Test and Screen
18. Ship, Inventory

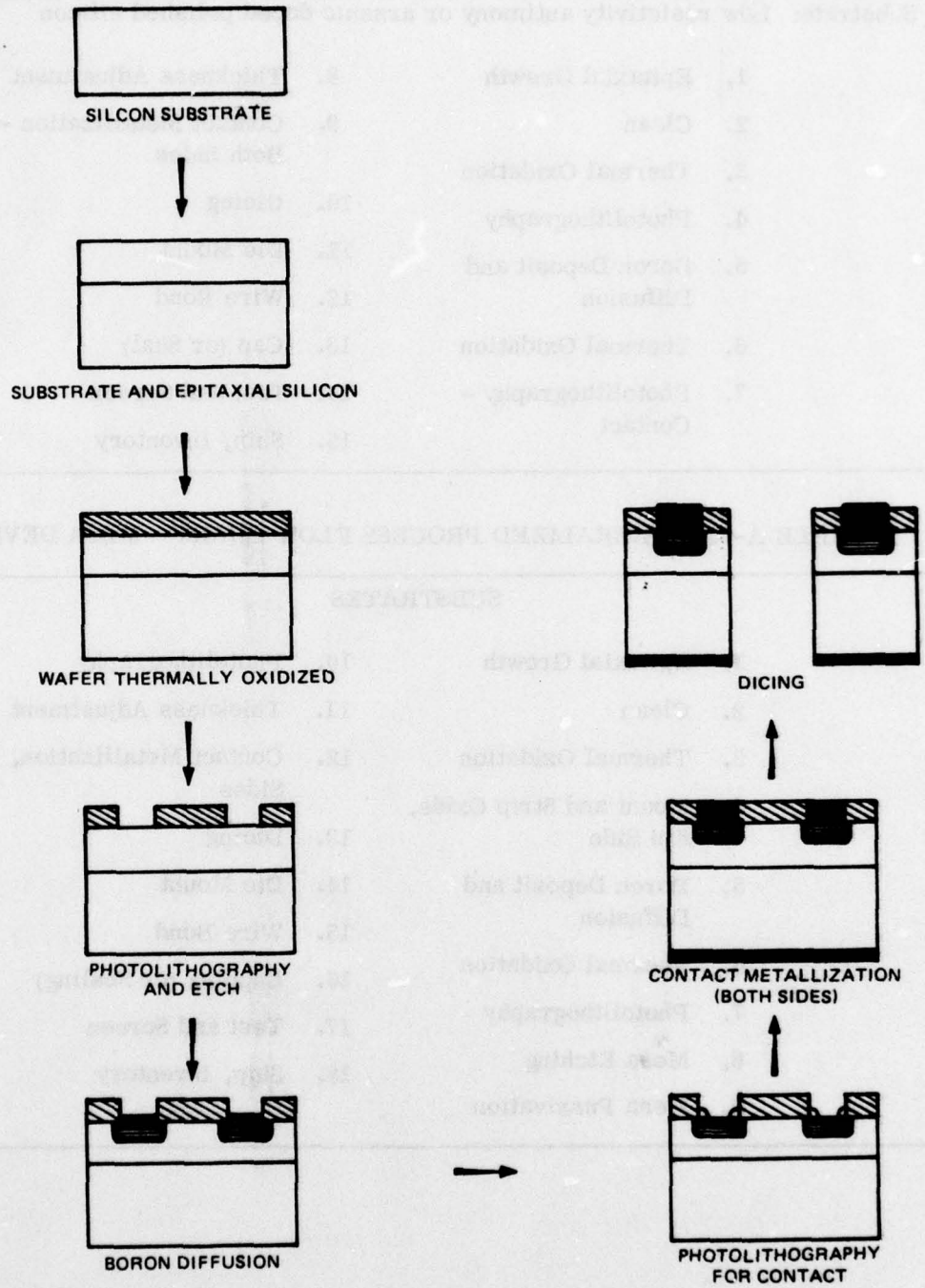


Figure A-3. Typical Process Sequence, Planar Chips

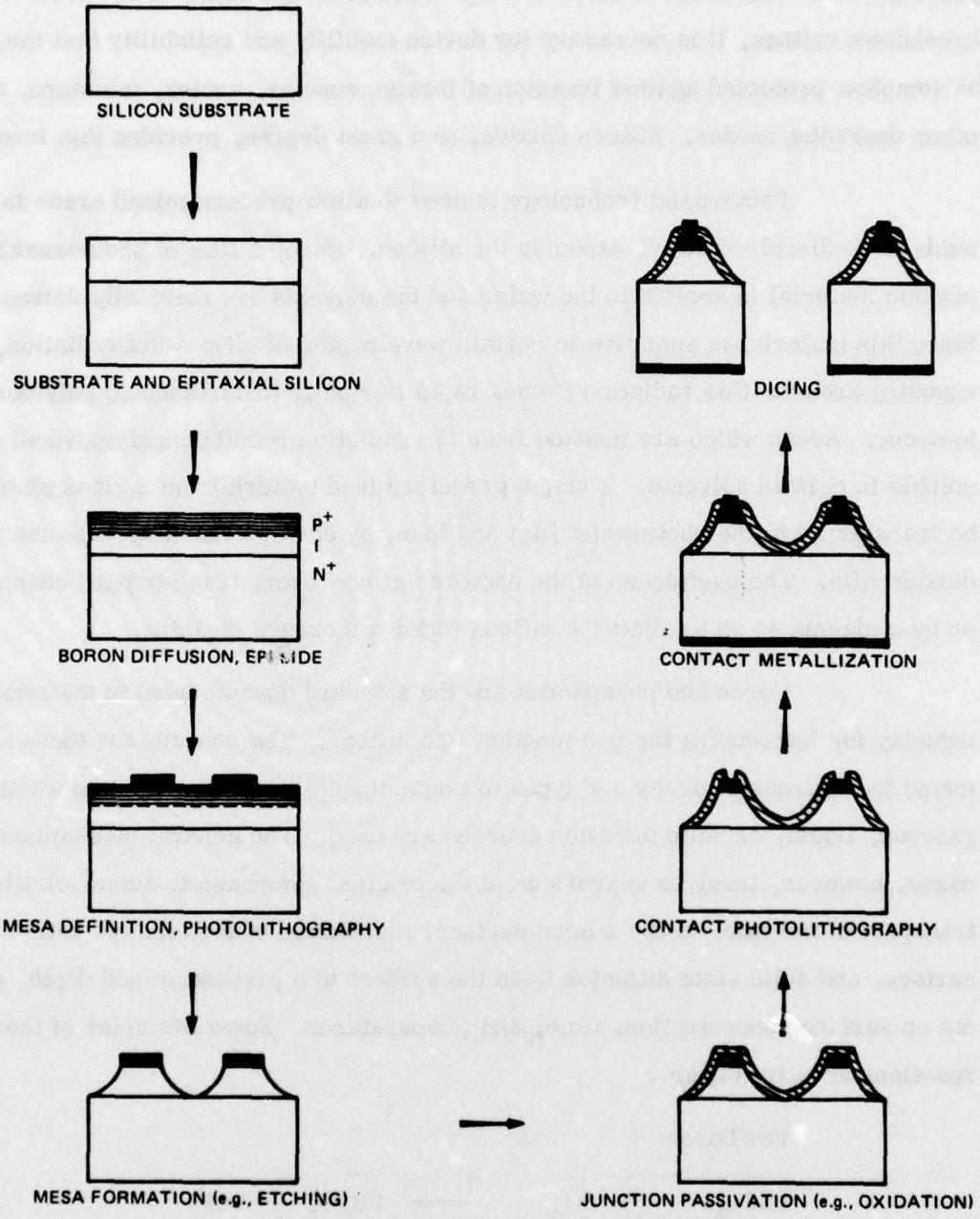


Figure A-4. Typical Process Sequence, Mesa Chips

junction. Since the electric field at the junction is on the order of 10^6 volts/cm at the breakdown voltage, it is necessary for device stability and reliability that the junction be somehow protected against invasion of foreign species, arcing, moisture, and other degrading modes. Silicon dioxide, to a great degree, provides this function.

Photoresist technology is used to allow predetermined areas in the oxide to be dissolved away, exposing the silicon. Here, a film of photosensitive organic material is applied to the wafer and the solvents are thermally driven out. Since this material is sensitive to certain wavelengths of ultraviolet radiation, exposing areas to this radiation causes rapid (virtually instantaneous) polymerization to occur. Areas which are masked from the radiation remain unpolymerized and soluble in certain solvents. Thus, a predetermined pattern from a glass plate can be transferred to the photoresist film and then, by chemical etching, into the silicon dioxide film. The usefulness of the photoresist now over, it is stripped chemically or by a plasma so as to allow the silicon wafer a thorough cleaning.

Boron and phosphorus are the standard dopants used in the microwave industry for introducing the p–n junction into silicon. The sources for these are many; the degrees of purity and types of contaminants vary depending on whether gaseous, liquid, or solid diffusion sources are used. The general mechanism in all cases, however, involves conversion of the original compound to some volatile oxide, transport of the oxide to the silicon surface, dissolution of the element within the surface, and solid state diffusion from the surface to a predetermined depth, dependent on surface concentration, time, and temperatures. Some examples of the doping reactions are given below.

For boron:

$$4BCl_{3\,(gas)} + 3O_2 \longrightarrow 2B_2O_3 + 6Cl_2$$

$$2B_2H_{6\,(gas)} + 3O_2 \longrightarrow 2B_2O_3 + 12H_2$$

$$4BBr_{3\,(liquid)} + 3O_2 \longrightarrow 2B_2O_3 + 6Br_2$$

$$4BN_{solid} + nO_2 \longrightarrow 2B_2O_3 + \text{oxides of nitrogen}$$

then

$$2B_2O_{3_{(gas)}} + 3Si_{(solid)} \longrightarrow 3SiO_{2_{(solid)}} + 4B_{(solid)} + \text{doped oxide}$$

and

$$B_{surface} \longrightarrow B_{bulk_{(substitutional)}}$$

For phosphorus, analogous reactions occur:

$$2POCl_{3_{(l)}} + \frac{3}{2}O_2 \longrightarrow P_2O_5 + 3Cl_2$$

or

$$2PH_{3_{(gas)}} + \frac{3}{2}O_2 \longrightarrow P_2O_5 + 3H_2O$$

then

$$2P_2O_5 + 5\,Si \longrightarrow 5\,SiO_2 + 4P \text{ doped oxide}$$

finally,

$$P_{surface} \longrightarrow P_{bulk_{(substitutional)}}$$

Mesa etching is a chemical step in which the selective dissolution of silicon is carried out. Usually, silicon etches for mesa formation are mixtures of nitric and hydrofluoric acids, wherein the mechanism of the reaction involves oxidation of the silicon and subsequent dissolution of the oxide by the hydrofluoric acid present. Occasionally acetic acid is used as a reaction moderator, affecting the degree of ionization of the nitric acid present.* The overall reaction can be considered to be:

$$3\,Si_{(solid)} + 12\,HF + 4\,HNO_3 \longrightarrow 3\,SiF_{4_{(aqueous)}} + 4NO_{(gas)} + 8\,H_2O_{(aqueous)}$$

*H. Robbins and R. Schwartz, J Elec. Soc. Vol. 107, No. 2, pp. 108-111

Areas are preselected for etching by exposing the silicon surface to the action of the etchant. Areas not to be etched are said to be masked against the etchant; masking can be affected by photoresist, thermal oxide, silicon nitride or certain waxes. The depth of the etch is usually measured by mechanical means (e.g., micrometer) and can be controlled electrically by both measurement of V_B and capacitance at some bias voltage.

Metallizations can be performed either wet or dry, by plating or by vacuum techniques. Filament evaportation, RF and DC sputtering, electron beam evaporation are all useful in metallizing wafers. Problems can occur even at this stage of processing due to foreign chemicals in the plating baths, co-deposition in the evaporation or sputtering, and radiation damage in RF sputtering to name a few. From a control point of view, contact resistance and adhesion are the prime considerations of a metallization scheme. Reliability (mean-time-before-failure) with respect to metallization dictates the type of metal(s) used, and contact resistance and adhesion dictates the method of applying these to the silicon.

Dicing silicon wafers can be done in several ways, among them sawing, scribing, laser cutting, and etching. Since, at this stage, no further high temperature processing will occur, there is concern now only for the surface condition of the silicon. Voltage breakdown and capacitance are affected by surface contamination on the chip. Lifetime and reliability can be affected by microcracks or saw damage propagating into the active area of the chip. Bonding can be prevented by even a monolayer of impurities on the contact metallization surface. A good indicator of surface condition and one which is used frequently to test diodes, is a high temperature reverse bias condition, for a prolonged period of time, monitoring leakage current. Contamination on the chip will be observed as an increasing leakage current with time, and premature device failure. Well-passivated, clean, non-contaminated chips often have leakage currents of less than a nanoampere before and after reverse bias at elevated temperature.

It is at this stage in the process when chips are assembled into diodes. Die mounting, wire bonding, or strapping and encapsulation, either by sealing or capping, are relatively lower temperature operations than the chip has seen earlier and, usually, surface contamination would be the prime reason for failure.

A.1.1.2.4 Chemicals Used

During these process steps, the more highly controlled silicon slices encounter any or all of the less controlled chemicals listed in Table A-3. Combining with these chemicals are the high temperature operations necessary to provide reasonable times for the solid state dissolution and diffusion of controlled amounts of impurities. It now becomes evident that any of these chemical or thermal interactions with the silicon wafers provides possible ingress to an unwanted species, leading to premature device failure.

Chemicals used in the fabrication of silicon microwave devices encompass the three physical states of materials: solids, liquids, and gases. Solid chemicals are normally zone refined and analyzed for impurities. Liquid chemicals are specified as electronic or MOS grade by most suppliers. These are normally analyzed wet chemical techniques complemented by atomic absorbtion or emission techniques. The analyses for the particular lot are not reported but are guaranteed to be written specified maximum values. The analyses are generally inorganic, covering metal species, nitrates and sulfates, as well as chlorides.

The specification of impurity levels by maximum permissible levels rather than actual measured levels opens the possibility that, from lot to lot, actual amounts of metallic impurity may, and probably do, vary within the manufacturer's specification. One particular lot might contain two parts per billion of sodium, while the next might contain 200 parts per billion; both lots, however, meeting the supplier specification of 15 parts per million maximum. The variation in the actual amount of contaminant from lot to lot could be sufficient to cause wild fluctuations in the silicon process yields from run to run. In addition, since the highly purified chemicals are routinely used in batch amounts, either in pure form, mixed with other acids, or diluted with deionized water, other avenues of contamination are possible. The

cleanliness of the reaction vessels, which are usually cleaned in similar chemicals and rinsed in the same deionized water, is essential.

TABLE A-3. LESS CONTROLLED CHEMICALS

Acids	Solvents	Aqueous
Hydrofluoric	Methanol	DI Water
Hydrochloric	2-Propanol	Plating Solutions
Acetic	Xylene	Metal Etches
Nitric	Benzene	
Sulfuric	Trichloroethylene	
	Methylene Chloride	
	Methyl Ethyl Ketone	
	Acetone	
Gases	**Liquids**	**Solids**
Hydrogen	Phosphorus Oxychloride	Waxes
Argon	Boron Tribromide	Abrasives
Nitrogen		Boron and Phosphorus Compounds
Oxygen		
Silane		
Diborane		
Phosphine		
Hydrogen Chloride		

Water is necessary at most points in the process for cleansing or rinsing operations and has to be extensively purified before usage. Raw city water, either from wells or reservoirs, is typically filtered, upgraded by any of several methods including reverse osmosis and dialysis, and finally polished to the theoretical limit of purity for the measured temperature usually reaching 18 megohms at 25°C. The final stage of purification is normally an ion exchange technique, followed by sub-micron filtering and ultraviolet sterilization. Final polishing stations may be located at the outlet locations to insure no degradation of the water in the delivery

lines. In addition, frequently monitoring the counts of bacteria present in the more stagnant drops insures that a high quality water will be delivered to all stations. Chemical sterilization can be used in the system when or if bacteria counts rise to an unacceptable level. Thus, the process water is considered to be as clean and impurity-free as is possible for liquid phase systems. To say this quantitatively, however, has not been possible until only recently with the advent of sub-trace quantitative and qualitative analytical tools.

Finally, the gases used in device fabrication are generally ultrapure. Where possible, liquid sources are used, in close proximity to the process laboratory. Gas delivery is via stainless steel tubing which has been thoroughly pressurized and leak checked.

A.1.1.2.5 Critical Areas of Processing and Control Points

Those areas of the wafer processing which are the most critical are those which involve processing at elevated temperatures. These areas, the formation of the thermal oxide and the formation of the p-n junction, are critical to the proper operation of the device. Even more importantly, the areas provide the conditions under which any contamination of the surface of the wafer or the mesas, from cleaning or etching procedures or contaminated ambient conditions, can be incorporated into the finished device.

The properties of the thermal oxide are evaluated both physically and electrically. The physical characterization involves the measurements of thickness and pinhole density.

For oxide thickness measurement, a test monitor accompanies the lot being processed; this monitor is measured by either a fringe count, or by ellipsometry, to determine the thickness. Pinhole density (or film integrity) can be measured by immersing the wafer in a suitable electrolytic cell as the cathode, and observing (and counting) the sites where H_2 evolution occurs by cathodic reduction. Normally, the anode is a noble metal, although copper could be used, for permanently "decorating" the pinhole site with copper, attracted to the cathodic site and reduced only at that site.

Electrically, the quality of the oxide film can be determined by borrowing from the MOS technology the determination of the shift in the flat band voltage caused by mobile and immobile charged species and interfacial states trapped in the oxide film. Sodium ion, incomplete silicon-oxide bonds, hydrogen ion and other impurities result in charges in the oxide, in the order of $1 \times 10^{10} - 1 \times 10^{12}$ charges/cm^2. Some of these charges are mobile with temperature and electric field, and cause inversion layers in silicon. These inversions lead to reduction in breakdown voltage, instability in leakage current, and tuning problems such as post tuning drift. Furnaces are monitored for variations in flat band voltage shifts and bias stressing at elevated temperatures, and when shifts occur beyond some acceptable value, the quartzware is either cleaned or replaced. HCl gas has been found to reduce Q_{ss} levels (lesser flat band shifts) in silicon dioxide films when incorporated in the film, as well as provide adequate cleaning of furnace tubes by reacting with sodium and other species migrating through the quartzware and carrying them off in the vapor phase.

Controls in the formation of the p-n junction are also used at this point in the process. The delivery ability of the doping system is monitored within each run by measuring the sheet resistance of the silicon by way of a four-point probe measurement, either on a test monitor or on a test pattern on the actual patterned wafer. The sheet resistance is directly related to the concentration of dopant in the surface of the wafer, and the depth to which it is diffused. In addition, the actual depth can be measured (in a test monitor) by angle lapping and staining the junction. Fringe counts (e.g., thallium light) can be used to arrive at the actual junction depth. The integrity of the junction, as well as the type of junction, can be measured electrically at this process point. Voltage breakdown and capacitance voltage relationships can be determined. The "abruptness" or degree of "gradedness" of the junction can be readily determined from the CV relationship. The quality of high resistivity I-region in a PIN slice after processing can be observed in the "reach through" (or punch through) voltage. The lower the punch through voltage, the higher the resistivity, for a given thickness of I-region. Finally, the gradedness of the interface between the high and low resistivity silicon can be seen from the CV characteristic, appearing as a more negatively sloped plot for the graded interface, and a flatter plot for the

more abrupt interface. Minority carrier lifetime to a first approximation can also be measured at this point, provided one can obtain good contact between the probe and the wafer. This measurement is normally a pulse measurement between forward and reverse bias and is observed on a sampling oscilloscope. The measurement can provide information on the later performance of the diode from an R_s point of view, as well as indicate problems in the process, either thermal or chemical.

One example might be cited: prior to a high temperature thermal oxidation, a silicon wafer, designed to provide microwave limiter chips (e.g., for a TR duplexer) is subjected to a stringent cleaning operation. Unknown to the operator, metallic contamination, gold, is present in one of the acid solutions used for cleaning. The concentration need only be a few parts per billion. The mechanism of ingress can then be pictured:

a. Diffusion of gold contaminant to silicon surface.

b. Physical or chemical absorption onto surface, in a concentration satisfying the equilibrium distribution with the solution.

c. Solid state diffusion of the contaminant, either substitutionally or interstitially, into the silicon lattice during the high temperature processing stage.

During this step, the concentration of contaminant in the bulk will be determined by the surface concentration, time and temperature, and the solid solubility of the contaminant at the given temperature.

These contaminant atoms are now frozen in the crystalline lattice, where their effect will be to provide trapping centers for minority carriers, drastically decreasing minority carrier lifetime. This phenomenon has a marked influence on the series resistance of the chip which will be observed as increased insertion loss for the diode and usually signifies the loss of the wafer. However, because insertion loss is not meaningful at this point in the process, the wafer would continue through the dicing operation, then progress to die mounting, wire bonding and capping. All the while, manufacturing costs are being accumulated for this particular wafer, for which no return will be observed. The indicator, of course, during wafer processing,

is the measurement of lifetime. But even where the wafer is discarded at that point, the question would trouble many a process engineer: why the low lifetime for this material? Is it contamination, and if so, what, and from where? Has anything else become contaminated because of it?

A.1.2 Microwave Device Theory and Design

This section will present a generalized approach to microwave device theory and design concentrating on two types of devices only: PIN diode and tuning varactor. The approach will emphasize general principles of design and associated performance, design parameters, optimized and practical designs, the effect of extraneous conditions (such as material defects, process deficiencies, wrong assembly techniques, etc.) on the device performance.

A.1.2.1 PIN Diode - A PIN diode is a semiconductor device which controls power in a microwave circuit. Power control is achieved in the form of switching and/or attenuation; and it is accomplished by presenting to the circuit an "open" circuit - "short" circuit combination and/or variable insertion loss behavior, respectively. The PIN diode is ideally suited for such power control functions as under reverse bias it will be a low-loss reactance (with very small capacitance) and under forward bias a very small resistor.

The design theory presentation in this subsection will be made in a form which relates the physics of the device to the performance parameters vis a vis environmental properties influenced during processing. The approach will be general inasmuch as understanding of these relationships is concerned; that is, specialization will occur only when it helps in understanding the properties of the device.

The theory will describe the free-carrier behavior as this is the stepping stone to the full realization of device parameters. The things that influence and are associated with these parameters will, therefore, also be elucidated.

A.1.2.1.1 Minority Carrier Model

If the intrinsic region is assumed to be truly "intrinsic," then the analysis of the minority carriers become meaningful under forward bias. This is

because only under forward bias is there any appreciable amount of minority carrier present in the I-region.

We start with the current-continuity equation for holes:

$$\frac{\partial p}{\partial t} = -\frac{p}{\tau_p} - \frac{1}{e}\nabla J_p \tag{1}$$

where p is the hole concentration and J_p is the hole current density. Noting that

$$J_p = -e D_p \nabla_p \tag{2}$$

we derive for the steady state $\left(\frac{\partial p}{\partial t} = 0\right)$ and one-dimensional cases:

$$\frac{d^2p}{dx^2} - \frac{p}{\tau_p D_p} = 0 \tag{3}$$

The same formulation for the electron concentration, n, results in:

$$\frac{d^2n}{dx^2} - \frac{n}{\tau_n D_n} = 0 \tag{4}$$

One point of paramount importance must be noted here. The I-region must obey the charge neutrality law at every point. Therefore

$$n(x) = p(x) \tag{5}$$

This condition will impose severe rules on electrons and holes as far as the recombination mechanism is concerned. We shall see this more clearly, later.

The solutions to Equations (3) and (4) are of the form

$$p = Ae^{\frac{x}{L_p}} + Be^{-\frac{x}{L_p}} \tag{6}$$

$$n = Ce^{\frac{x}{L_n}} + De^{\frac{x}{L_n}} \tag{7}$$

where

$$L_p = \sqrt{\tau_p D_p} \quad \text{and} \quad L_n = \sqrt{\tau_n D_n}$$

A, B, C and D are constants to be determined by the boundary conditions. The prime boundary condition is, of course, Equation (5) which dictates that

$$L_p = L_n = L$$

and

$$A = C$$

$$B = D$$

The other boundary condition is that

$$p(o) = n_i \, e^{\frac{qV_F}{kT}} = n(W_I)$$

at sufficiently high forward bias. With these boundary conditions the solution becomes

$$p(x) = n(x) = n_i \, e^{\frac{qV_F}{kT}} \left\{ \frac{1 - e^{-\frac{W_I}{L}}}{2 \sinh\left(\frac{W_I}{L}\right)} e^{\frac{x}{L}} + \frac{e^{\frac{W_I}{L}} - 1}{2 \sinh\left(\frac{W_I}{L}\right)} e^{-\frac{x}{L}} \right\} \quad (8)$$

The graphical representation of this equation is shown in Figure A-5. Equation (8) will be valid even when the I-region is not quite "intrinsic." In fact, the mathematical difference for the forward bias case between 100 and 10,000 ohm · cm is negligible. Equation (8) is also valid for any W_I/L ratio.

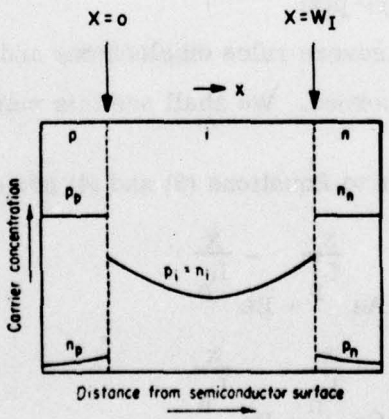


Figure A-5. Typical Carrier Distribution in i Layer of p-i-n Diode under Forward Bias. The p Layer, i Layer, and n Layer Are Assumed To Be Uniformly Doped, with Abrupt Transitions in Doping between Layers. Carrier Densities p, and n Are Densities in the Presence of Injection, rather than Intrinsic Carrier Densities.

A.1.2.1.2 Calculations of Diode Impedance

The imposed conditions on recombination mechanism, as we have seen above, dictated that

$$T_p = T_n = T \tag{9}$$

This enables us to safely assume an ambipolar mobility μ_{A_p} which is

$$\mu_{A_p} = \frac{2\mu_p\mu_n}{\mu_p+\mu_n} \tag{10}$$

Conceptually this μ_{A_p} which is about 610 cm^2/VS in silicon is the effective average of the hole and electron mobilities.

With these assumptions we can now calculate the forward bias resistance, R_I. Note that

$$R_I = \frac{W_I}{\sigma A} = \frac{W_I}{Aq\left(\mu_p p + \mu_n n\right)} = \frac{W_I}{2q A\mu_{Ap} p} \tag{11}$$

But the injected charge Q_p, is directly proportional to the forward bias current.

$$Q_p = qp\ A\ W_I = I_F\tau \tag{12}$$

Combining Equations (5), (12) and (11) yields

$$R_I = \frac{W_I^2}{2\mu_{Ap} I_F\tau} \tag{13}$$

As can be seen, R_I is independent of diode area, A, but inversely proportional to lifetime and bias current. Since this equation is very widely used, a few words of caution are in order:

(a) We don't necessarily keep R_i constant by changing A because, generally speaking, I decreases with a decrease in A. This is due to I-region carriers now being nearer to the periphery where recombination can occur more rapidly.

(b) R_I decreases with I_f so long as τ remains constant. It should be recognized that as I_f increases, carrier density increases, and the recombination

probability increases, decreasing τ. Furthermore, saturation is reached when p and n increase sufficiently so that substantial injection (holes into the n^+ region and electrons into the p^+ region) becomes significant, further increasing recombination probability. Put simply, if there are high densities of electrons and holes in the I-region, their chance for recombining increases, decreasing the average lifetime.

During reverse bias the impedance will not only have a resistive component (as in the forward bias case) but also a reactive component which will actually dominate the diode behavior after punch-through. The study of the reverse bias necessitates the use of finite resistivity for reasons of realism. Now, we start with Poisson's Law

$$\frac{dE}{dx} = \frac{q}{\epsilon} N_a \tag{14}$$

Integrating Equation (14) and applying the boundary condition that the electronic field, E, vanishes at W

$$E = \frac{q}{\epsilon} N_a (W-x) \tag{15}$$

A second integration over the same depletion region gives the junction voltage, $V_j = -V_a + V_d$ (where $-V_a$ is the applied reverse bias and V_d is the built-in voltage).

$$V_j = -V_a + V_d = \frac{q}{\epsilon} N_a \frac{W^2}{2} \tag{16}$$

This gives us the standard formula relating depletion width, W, to applied potential.

We can now calculate the values of C_j, C_i, X_j, X_i, R_j and R_i. These elements are depicted in Figure A-6. Since R_j is very large compared to X_i it is quite safe to approximate the total impedance of the I-region by

$$Z = R + jX \approx j \left(X_j + \frac{X_i R_i}{R_i + jX_i} \right) \tag{17}$$

Expressions for C_j, C_i and R_i are

$$C_j = \frac{\epsilon A}{W}; \; C_i = \frac{\epsilon A}{W_I - W}; \; R_i = \frac{\rho}{A} W_I - W \tag{18}$$

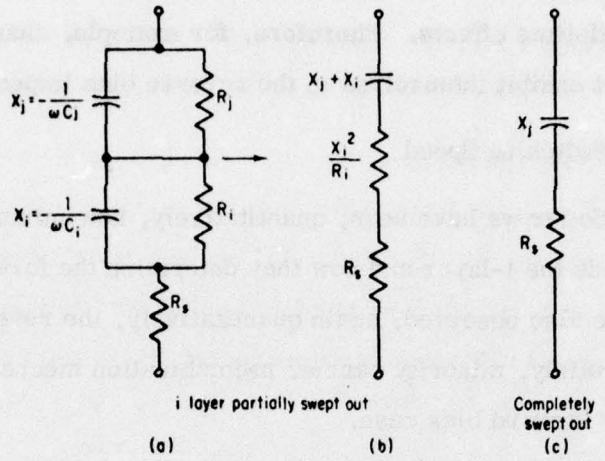


Figure A-6. Approximate Equivalent Networks for p-i-n Diodes under Reverse Bias at Microwave Frequencies

Substituting (18) into (17) gives us the series resistance and reactance of the I-region

$$R_s = \frac{\rho\left(W_I - W\right)}{A\left(\rho^2 W^2 \epsilon^2 + 1\right)} \quad \text{and} \quad X = \frac{-\rho^2 W \epsilon}{A\left(\rho^2 W^2 \epsilon^2 + 1\right)} \left(W_I + \frac{W}{\rho^2 W^2 \epsilon}\right) \tag{19}$$

If $\rho W \epsilon >> 1$ (as is the case for a good microwave PIN device), we can approximate the resistance and reactance as

$$R \approx \frac{W_I - \left[2\epsilon\mu\rho\left(-V_a + V_d\right)\right]^{1/2}}{W^2 \; {}^2A} \quad \text{for} \quad 0 \geq V_a \geq V_d - \frac{W_I^2}{2\epsilon\mu\rho}$$

$$R = 0 \quad \text{for} \quad V_a < V_d - \frac{W_I^2}{2\epsilon\mu\rho}$$

$$X \approx \frac{-W_I}{W\epsilon A} \tag{20}$$

The above analysis has shown that if the operating frequency and the I-region resistivity are high, the capacitance of the I-layer is independent of the bias voltage and is equal to that of a parallel-plate capacitor of separation W_I and plate area A. It has also been shown that the resistance of the I-region decreases with increasing bias voltage, V_a, as well as with increasing operating frequency, I-layer resistivity and permittivity. Furthermore, it is obvious from Equation (20) that reverse bias

impedance measurements, no matter how accurately they may be performed, are insensitive to lifetime effects. Therefore, for example, changing conditions in the process will not exhibit themselves in the reverse bias impedance parameters.

A.1.2.1.3 Switching Speed

So far we have seen, quantitatively, how minority carriers are distributed inside the I-layer and how they determine the forward resistance of the diode. We have also observed, again quantitatively, the reverse bias behavior of the diode. Certainly, minority carrier recombination mechanisms play a first order role only in the forward bias case.

If one is to study surface effects it is important to identify as many mechanisms as possible which are influenced by surface recombination so that independent inputs are provided for analysis of the surface conditions. Even though switching speed, at first glance, appears as one such possibility, a closer look states otherwise. A properly designed driver circuit can artificially "suck-out" the stored charge. Hence, switching speed can be made to vary over a range even with the same lifetime inside the PIN diode. A better measure of the switching speed is really the transit time of the carriers through the I-region by the diffusion process.

The average transit time, t_w is given by

$$t_w = 0.038\ W^2 \tag{21}$$

Hence, the transit time is only dependent on I-region thickness and not lifetime.

It is, therefore, necessary to look for some other parameter to provide us with information on changing surface conditions. Note that

$$\frac{1}{\tau} = \frac{1}{\tau_s} + \frac{1}{\tau_b}$$

where τ_s is the surface recombination life-time and τ_b is that of the bulk. Recognizing that the reverse saturation current density, J_s is dependent on τ:

$$J_s \sim \frac{D_n}{L_n} + \frac{D_p}{L_p}$$

$$\sim \frac{1}{\sqrt{\tau_n}} + \frac{1}{\sqrt{\tau_p}} \tag{22}$$

Thus, the possibility of looking at reverse leakage current, particularly close to avalanche, to identify deviations from the ideal conditions on the surface appears quite real, as we will elaborate on in subsections A.1.5 and A.1.7. We propose to observe this J_s over a long time span at high temperature to deduce meaningful information on the surface degradation.

A.1.2.2 Tuning Varactor - A tuning varactor is a device which, in most applications, changes the output frequency of an oscillator with applied dc bias. Its major function, therefore, is to present a certain variation of capacitance with voltage to a tank-circuit. What is required of a tuning varactor, in microwave applications, is, of course, much more complex. In the first place, every time the applied voltage varies a certain way, the capacitance should vary the same way. In other words, no hysteresis effect is allowed as this would engender different resonant frequencies for the same bias. Secondly, the capacitance of the diode at a given bias should be invariant in time. Namely, the resonant frequency is not allowed to drift (even 0.1% in some cases). More comment on this drift problem will be presented in subsection A.1.5. Additionally, the diode should absorb an incident power minimally and the amount of the absorbed power should not change with time. This means that the quality factor, Q, of the diode should be high (for low insertion loss) and should remain constant, as a variable load would otherwise produce instability in the circuit. In summary, it is totally insufficient to manufacture a semiconductor device performing to specifications indicated by the semiconductor theory because the device is not just a semiconductor chip but an integral part of a microwave system. Accordingly, we will present the most appropriate theory and design applicable to microwave tuning varactors but with an eye to the eventual application of the device in the system.

A.1.2.2.1 General Principles

The most general approach to tuning varactor design is to assume an abrupt junction case but with a doping profile N(x) in the epitaxial layer varying exponentially:

$$N(x) = N_0 e^{kx} \quad cm^{-3}$$

where N_0 is the doping concentration at the surface (X = 0) in atoms/cm^3 and k is the doping gradient factor in cm^{-1} (or μ^{-1}). The reason for such generalization is as follows:

a. To maximize Q, the epitaxial layer thicknesses used in microwave tuning varactors are in the range of 3-10 micrometers. Hence, the diffusions in these epi layers are necessarily quite shallow (<2 microns). This invariably results in an abrupt junction the depletion into which is four to five orders of magnitude less than that into the epi layer. Therefore, no measurable error will be incurred by assuming that all the depletion is into the epi layer.

b. The doping profile in the epi layer is not as constant as it is usually assumed. This problem, which emanates mostly from the out-diffusion of dopants from the substrate and/or poor injected dopant control during the epitaxy deposition process, has the effect of changing the capacitance-voltage dependence and therefore plays a first order role in the device performance. Also, it is important to distinguish, for diagnostic reasons, the influence of a doping profile's non-constancy from the influence of ionic surface contamination on the device performance. Besides, a constant doping profile case can easily be analyzed by merely making k = 0. Thus, the added complexity (which is only algebraic) is compensated by useful generality.

We start our analysis by noting that:

$$\frac{d}{dx}(xy) = x\frac{dy}{dx} + y \tag{1}$$

If y is taken to be the electric field, E, then we can pursue this line of thinking by further noting that

$$\frac{d}{dx}\left(x\frac{dv}{dx}\right) = x\frac{d^2v}{dx^2} + E \tag{2}$$

Recognizing that the field, E, $(\frac{dv}{dx})$ is approximately zero just beyond the boundaries of the depleted region and integrating both sides of Equation (2) over the length of the depletion region, one finds that

$$\int_0^W \frac{d}{dx}\left(x\frac{dV}{dx}\right)dx = x\frac{dV}{dx}\Big]_0^W \approx 0 = \int_0^W x\frac{d^2V}{dx}\,dx + \int_0^W E\,dx$$

Thus
$$\int_0^W E\,dx = V_j = V_a + V_d = -\int_0^W x\frac{d^2V}{dx^2}\,dx \tag{3}$$

We know, from Poisson's Equation that

$$\frac{d^2V}{dx^2} = -\frac{q}{\epsilon_r \epsilon_0} N(x) \tag{4}$$

Substituting

$$\boxed{V_j = \frac{q}{\epsilon_r \epsilon_0}\int_0^W x\,N(x)dx} \tag{5}$$

where

q = 1.6×10^{-19} coulombs

$\epsilon_{r\,0}$ = 0.96×10^{-12} f/cm for silicon

$N(x)$ = $N_d(x) - N_a(x)$

$N_d(x)$ = Number of donors per unit volume

$N_a(x)$ = Number of acceptors per unit volume

V_j = Total junction voltage

V_a = Applied voltage

V_d = Diffusion potential = $\frac{kT}{q}\ in\left(\frac{N(W_1)N(W_2)}{n_1^2}\right)$

W_1 = Width of depletion into the n region

W_2 = Width of depletion into the p region

W = Depletion width at V_j

Employing the generalized exponential relationship for the doping profile we finally obtain:

$$V_j = 1.67 \times 10^{-7} N_0 \int_0^W x\, e^{kx}\, dx \tag{6}$$

Equation (6) is the fundamental equation governing the tuning varactor.

The solution of Equation (6) is transcendental and it is given by:

$$V_j = \frac{1.67 \times 10^{-7} N_0}{k^2} \left[e^{kW} (kW-1) + 1 \right] \tag{7}$$

A.1.2.2.2 Design Parameters

Analysis of Equation (7) yields us all the necessary interrelationships between capacitance, voltage and doping profile. Namely,

$$V_j = f(C, N_0, k)$$

where C is the capacitance per unit area.

$$C = \frac{\epsilon_r \epsilon_0}{W} \tag{8}$$

Thus

$$V_j = \frac{1.67 \times 10^{-7} N_0}{k} \left[e^{\frac{k \epsilon_r \epsilon_0}{C}} \left(\frac{k \epsilon_r \epsilon_0}{C} - 1 \right) + 1 \right] \tag{9}$$

which is our $f(C, N_0, k)$.

Equation (9) is plotted in Figure A-7 for various values of k and for $N = 10^{15}$ atoms·cm^{-3}. Some representative values of k corresponding to slopes in doping profiles are presented in Table A-4.

Two important points should be noted:

a. The deviation from the square-root-law (represented by k = 0 line) is significant even for $k = 0.091\,\mu^{-1}$. At V_j = 30V, for example, capacitance has increased by 20%. Capacitance ratio, therefore, between C at 4V and C at 30V has decreased by 20%. Moreover, the percent increase in capacitance gets worse at higher voltages.

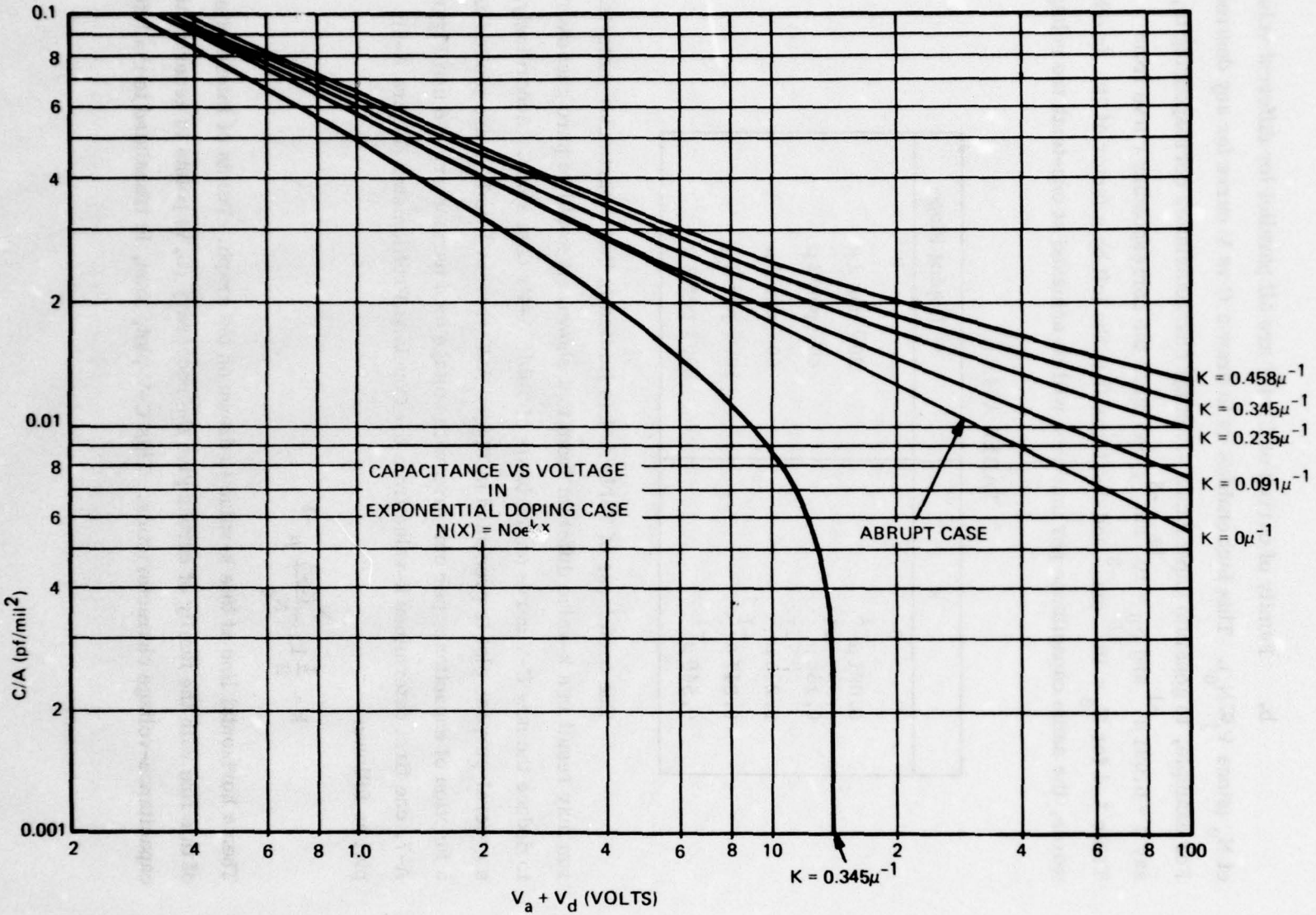


Figure A-7. Capacitance vs Voltage in Exponential Doping Case

b. Family of curves of C vs V are all parallel for different values of N_0 (since $V_j \propto N_0$). This fact enables us to draw a C vs V curve for any desired N_0. For example, to generate capacitance - voltage characteristics corresponding to, say $k = 0.091\,\mu^{-1}$ and $N_0 = 10^{14}\,cm^{-3}$, one takes the corresponding curve from Table A-4 for $N_0 = 10^{15}\,cm^{-3}$ and displaces it to the left by a factor of 10. In other words, the same capacitance per unit area will be achieved at one-tenth the voltage.

TABLE A-4.

k	Doping Slope
0	0
$0.091\,\mu^{-1}$	20% per 2 μ
$0.168\,\mu^{-1}$	40% per 2 μ
$0.235\,\mu^{-1}$	60% per 2 μ
$0.347\,\mu^{-1}$	100% per 2 μ
$0.549\,\mu^{-1}$	200% per 2 μ

The usefulness of Table A-4 is limited in that a particular material run may result in a k-value different from that shown. It would be pure guesswork to deduce the new C-V curve on the basis of Table A-4's data alone. Accordingly, a general-purpose plot is presented in Figure A-7 whereby k-values are plotted as a function of capacitance per unit area with voltage as a parameter. To use Figure A-7, one first determines k-value from the Copeland Profilometer (Figure A-8) plot as follows:

$$k = \frac{1}{2} \ln \frac{N_{(2\mu)}}{N_0}\ \mu^{-1}$$

Then a horizontal line at this k-value is drawn on the graph. Points of intersection of this line with the family of curves give the necessary (C, V) points to generate the capacitance-voltage characteristics. This C-V plot, then, is translated to the left

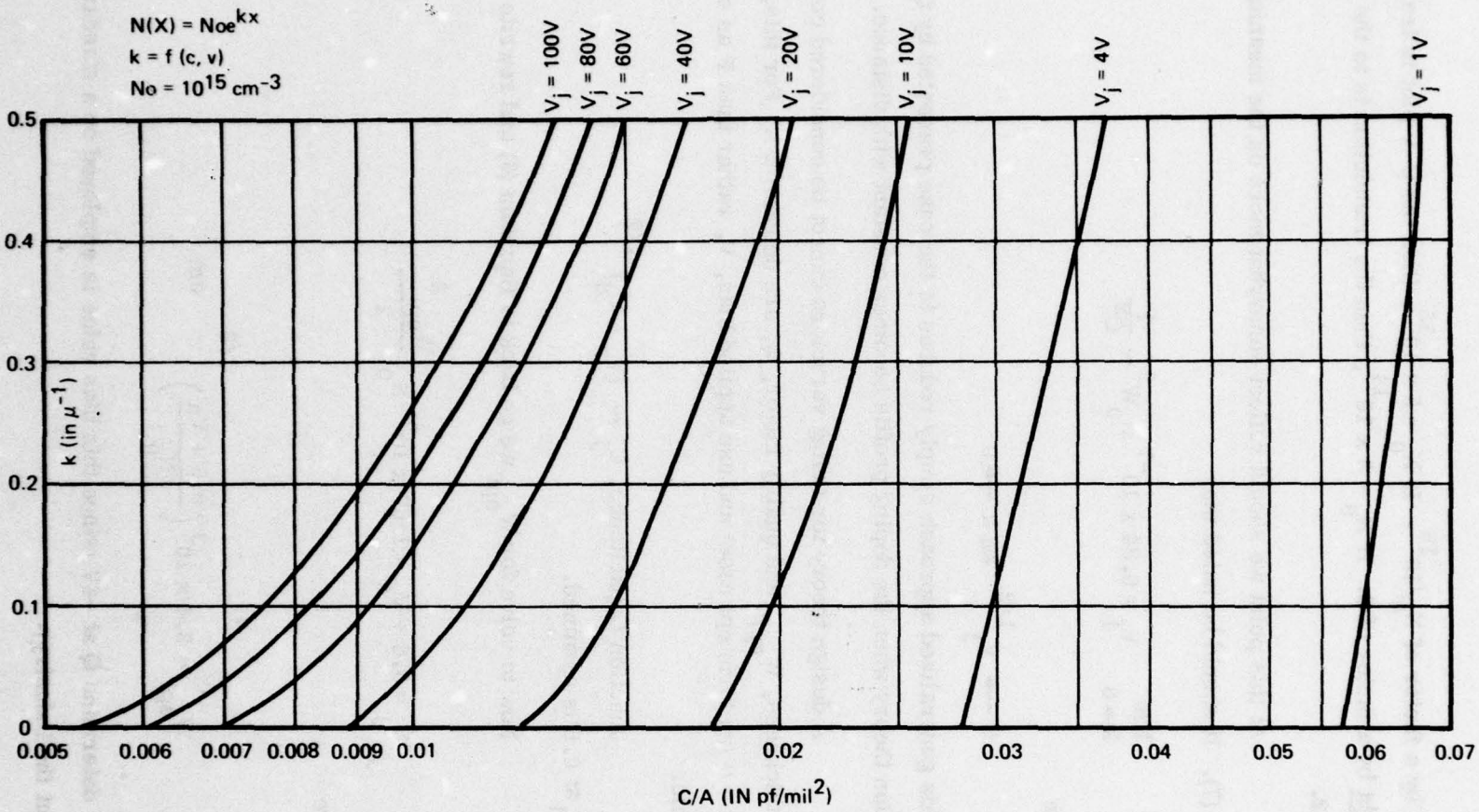


Figure A-8. Copeland Profilometer

(or right) by a factor of $N_0/10^{15}$. If $N_0 = 5 \times 10^{15}$, then the C-V plot is translated to the <u>right</u> by a factor of 5. If $N_0 = 5 \times 10^{14}$, then the translation is to the <u>left</u> by a factor of 2.

At this point we should reflect somewhat more on the meaning of Equation (7). It should be noted that

$$\lim_{k \to 0} \quad V_j = 0.84 \times 10^{-7} N_0 W^2 \sim \frac{1}{C^2} \tag{11}$$

Therefore

$$C \longrightarrow V_j^{1/2} \quad \text{as } k \longrightarrow 0 \tag{12}$$

Hence, this generalized approach simply reduces to the case presented by the standard p-n junction theory when the doping profile becomes constant with distance.

A design theory for tuning varactors cannot be considered complete until epi thickness, W_{epi}, and quality factor, Q, are determined. For this, we will assume k = 0 (uniform epi case) and use applied bias, V, rather than F as only F is measurable.

$$\text{Junction Capacitance, } C_j \sim (V_a + V_d)^{-1/2} \tag{13}$$

Where $V_d \approx 0.6$ is assumed.

Now to solve for W_{epi} we go back to Equation (6) and rewrite with k = 0

$$V_j = 0.6 + V_a = 1.67 \times 10^{-7} N_0 \frac{W_{epi}^2}{2} \tag{14}$$

Therefore

$$W_{epi} = 3.4 \times 10^3 \left(\frac{0.6 + V_a}{N_0} \right)^{1/2} \text{ cm} \tag{15}$$

Next, we determine Q at -4V (since this bias value is employed on a standard basis throughout the industry).

$$\frac{1}{Q_4} = \omega R_{S4} C_4 \tag{16}$$

Where $\omega = 2\pi f$

R_{S4} = Series resistance at -4V

C_4 = Capacitance at -4V

If the depletion width at -4 volts is W, then

$$R_{S4} = \frac{\rho}{A} \left(W_{epi} - W \right) \tag{17}$$

With ρ being the resistivity, and

$$W = 3.4 \times 10^3 \left(\frac{4.6}{N} \right)^{1/2} \text{ cm} \tag{18}$$

Also

$$\frac{C_4}{A} = 8.5 \times 10^{-10} \sqrt{N} \text{ pF mil}^{-2} \tag{19}$$

(Units have been chosen according to current engineering convention.)

Substituting Equations (19), (18) and (17) into (16) yields the formula for the quality factor. However, we shall present this formulation under two points of view in the following paragraphs.

A.1.2.2.3 Optimized Design

The concept of optimization will necessarily differ from system to system. Some systems may require maximum tunability with less regard to insertion loss. Some systems, on the other hand, may need only a token amount of tuning but with maximum possible quality factor. As a general case, here, we assume for the optimization procedure the simultaneous maximization of breakdown voltage, V_B, and quality factor, Q. This simultaneous maximization dictates that the diode avalanches as soon as it depletes fully. Thus, we need to develop the interrelationships between doping concentration, epi thickness and diode area and a given set of V_B, Q and C.

To be practical and useful we should limit ourselves to the ranges of common usage. Namely

$25 \leq V_B, \leq 300V$

$1X10^{15} < N < 3X10^{16}$ atoms $\cdot$ cm^3

$$300 \leq Q\ @\ -4V \text{ and } 50 \text{ MHz} \leq 13000$$

$$003 \leq C/A\ @\ -4V \leq 0.140 \text{ pF/mil}^2$$

The determining relationships, which have been all but completely developed in the above sections, can be written in the following form:

$$N = 2.143 \times 10^{18} V_B^{-1.33} \text{ atoms/cm}^3 \tag{20}$$

$$C/A = 8.5 \times 10^{-10} \sqrt{N} \text{ pF/mil}^2 \tag{21}$$

$$= 7.37 \times 10^{7} \rho^{-0.585} \text{ pF/mil}^2 \tag{22}$$

$$\rho = 2.84 \times 10^{13} N^{-0.855} \text{ ohm} \cdot \text{cm} \tag{23}$$

$$= 8.765 \times 10^{-3} (C/A)^{-1.71} \text{ ohm} \cdot \text{cm} \tag{24}$$

$$W_{epi} - (X_j + \text{Out diffusion}) = 0.0236\ V_B^{1.17} \text{ cm} \tag{25}$$

$$\frac{1}{Q_4} = 1.24 \times 10^{17} \left[N^{-1.2325} - 3 \times 10^{-7} N^{-0.855} \right] \text{ at 50 MHz} \tag{26}$$

A design nomograph combining all these parameters is presented in Figure A-9. Procedure for using the nomograph is simple. Breakdown voltage specification is entered on the leftmost column (under V_B). Then moving on a straight line toward the right we obtain the maximum allowed doping concentration, N_{max}. Continuing to the right gives us the theoretical maximum Q (at 100 MHz which is 0.5 times that at 50 MHz). Ideally, the Q specification is entered on the Q column and the minimum allowed value of N, N_{max}, is obtained. The range for N to be specified can then be judiciously chosen.

Now a range defined by the specified values of maximum N and minimum N is formed and it is continued straight to the right until it intersects the capacitance per unit area, C/A, column. Then the capacitance specification range (at -4V) is entered in the rightmost column. Finally, using straight lines, the

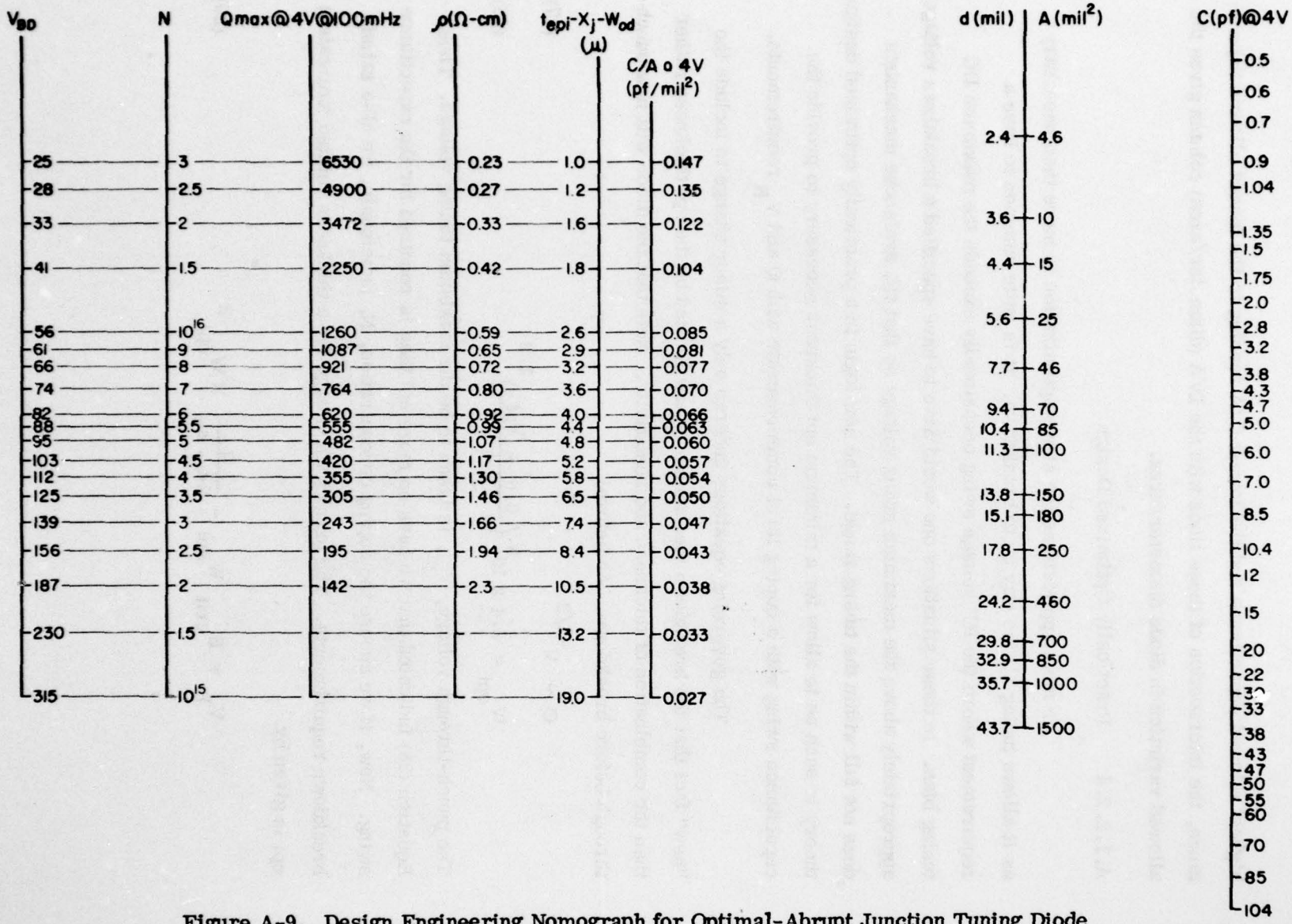


Figure A-9. Design Engineering Nomograph for Optimal-Abrupt Junction Tuning Diode

highest allowed capacitance and the lowest C/A reading to the lowest allowed capacitance, the intersection of these lines with the D/A (diameter/area) column gives the allowed variation in diode diameter/area.

A.1.2.2.4 Practically Optimized Design

In most applications the above optimization is more than necessary as it allows tuning all the way up to breakdown. It is quite common to have a requirement where the RF voltage swing occasionally exceeds the maximum DC tuning bias. In these situations one would have to have specified a breakdown voltage appropriately above the maximum swing voltage so that the avalanche mechanism does not fall within the tuning range. The new logic in a practically optimized design theory is such as to allow for a minimum epi thickness necessary to provide the capacitance swing with a doping level commensurate with Q and V_B requirements.

The governing equations undergo only a minor change to include the "new" fact that the breakdown mechanism is now limited by the epi thickness rather than the combination of thickness and resistivity. Note that the diode will now punch-through before breakdown. As before:

$$C \sim V^{-1/2} \tag{27}$$

$$W_{epi} = 3.4 \times 10^3 \left(\frac{0.6 + V_{pt}}{N} \right)^{1/2} \tag{28}$$

The punch-through voltage, V_{pt}, is taken to be the maximum tuning voltage. Thus, Equation (28) indicated that we have no more epi than is required for the capacitance swing. Now, if we choose the doping concentration, N, judiciously, we also satisfy breakdown requirements. The breakdown voltage for a thickness limited (truncated) epi is given by

$$V_B = E_{crit} W_{epi} - \frac{q}{2 \epsilon_r \epsilon_0} N W_{epi}^2 \tag{29}$$

where E_{crit} is the critical electrical field initiating the avalanche mechanism. This field is dependent on the ionization rate as well as mean free path before recombination. A very good empirical formula describing the actual situation is:

$$E_{crit} = 4.1 \times 10^{3} N^{0.125} \text{ V/cm} \tag{30}$$

Substituting Equation (30) into (29) and manipulating sufficiently we find the maximum allowed doping concentration, N_{max}.

$$N_{max} = 1.13 \times 10^{19} \left[\frac{(0.6 + V)^{0.5}}{V_B + 0.966 \left(0.6 + V_{pt}\right)} \right]^{2.667} \tag{31}$$

To obtain Q we combine Equations (18), (17), (19) and (16) and solve for minimum allowed doping concentration, N_{min}.

$$N_{min} = 4.18 \times 10^{11} \left[Q_4 \left(0.46 \sqrt{0.6 + V_{pt}} - 1 \right) \right]^{1.17} \tag{32}$$

A mid-point, for example, between N_{max} and N_{min} can be used in Equation (28) to determine W_{epi} required. An incorporation of all the parametric equations in a nomographical form is presented in Figure A-10.

To use the nomograph:

a. Start with the specified Q and go up vertically until the specified V-line is reached. The intersection point gives the minimum N we have to have to meet the specified Q and still have the required swing in capacitance.

b. All the way to the left is the capacitance per unit area that this N will give us at -4 volts. From this number and the specified C_4 we obtain the area of the diode.

c. Continuing horizontally to the right, we determine W_{epi} from the intersection of N-value and V-line.

d. All the way to the right we observe the theoretical breakdown. Also on the same graph we have an arbitrarily drawn experimental breakdown curve (broken line) depicting a particular passivation system. If the broken line is not coincident with the solid line then, obviously, compromise is necessary and the quality factor will suffer.

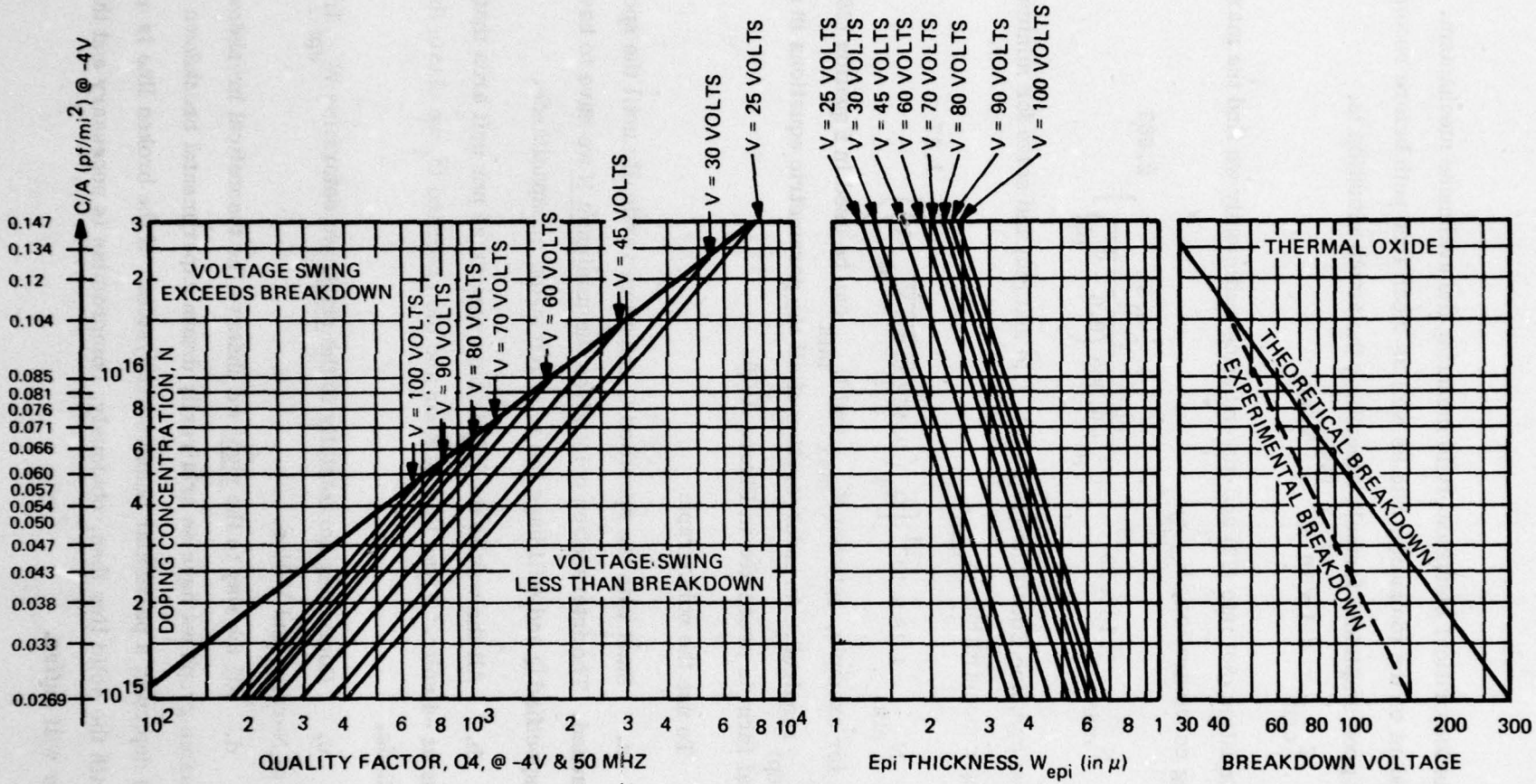


Figure A-10. Design Nomographs for Tuning Varactors with Truncated Epi

A.1.2.2.5 Deviations from Theoretical Behavior

As alluded to above, some deviations will occur from the predications given by theoretical analysis. This deviation almost always is in breakdown voltage. Apparently due to changes in the process conditions - most of which have remained unidentified - some degradation of the breakdown voltage occurs during the passivation step, utilizing, in particular, thermal oxidation. As an uncontrollable side effect of oxidation, uncompensated charged contamination is incorporated in the interface between the semiconductor and the oxide layer. The polarity of this charge is almost always positive in the case of oxide. Therefore, if the epi is n-type, an accumulation layer is produced on the surface modifying the conductivity there. The result is, of course, a degradation in the breakdown voltage. It should be noted in this regard that such surface-oriented degradation is not necessarily the course of every failure mode in the device but rather an indication of a non-ideal condition on the surface. Failure modes and their relationships to surface effects will be discussed in subsection A.1.5.

A.1.3 Detailed Processes - Fabrication of Microwave Diode Chips

a. PIN Diodes - The idealized doping profile of a PIN diode wafer is shown in Figure A-11.

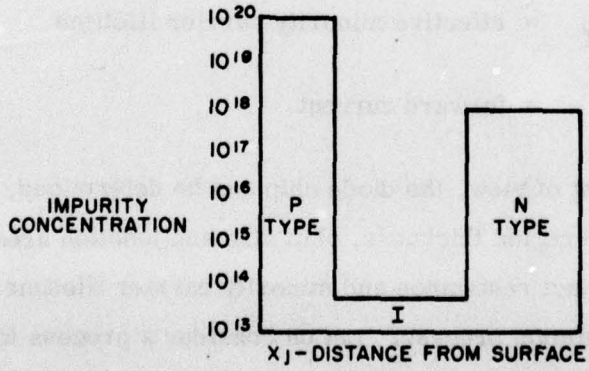


Figure A-11. Doping Profile

As can be seen, a heavily doped p-type region, and a heavily doped n-type region surround an "intrinsic" (more realistically, a slightly n-type) region whose volume determines many of the diodes' performance characteristics.

PIN diodes, depending on the application, whether a switch, attenuator, or limiter for example, are usually specified by voltage breakdown, capacitance (at zero bias, or some other bias voltage), R_s (at 10 or 100 mA), forward voltage, reverse leakage current, and lifetime. Chip size will be dictated by package considerations. The I-region thickness and junction depth will determine breakdown voltage, and the area of the junction and I-region thickness will determine the capacitance. Punch-through voltage is dependent on the resistivity and I-region thickness, and R_s will depend on the minority carrier lifetime, resistance of the swept out region, resistance of any residual unswept region, and contact resistances to the heavily doped n+ and p+ regions. If all other resistances are minimized (or negligible), the main contributor to the R_s for a PIN diode may be represented as

$$R_s \cong \frac{W^2}{2\mu \tau_{eff} I_f}$$

where

W = final I-region thickness

μ = effective mobility $\cong 600 \frac{cm^2 - volts}{sec}$

τ_{eff} = effective minority carrier lifetime

I_f = forward current

From a design point of view, the diode chip can be determined, then, by deciding on a certain final I-region thickness, chip size and junction area; the other parameters, such as contact resistance and minority carrier lifetime really are results of selection of the optimum process. Let us consider a process for fabrication of a microwave PIN switch. We have been presented a specification of the following type:

V_B at 10 μamps = 35 volts min

C_T (at -20 volts) = 1.0 pF max

T_L = 100 nsec max

R_s = 0.5 ohm max at 10 mA

Package style dictates a chip no larger than 30 mil^2. Gold metallization is preferred by the customer. One can measure the capacitance of an empty glass package and, after subtracting this from the total capacitance listed in the specification, one arrives at the design capacity value for the chip. A calculation based on the well-known equation

$$C = \frac{K\epsilon A}{W}$$

where

A = junction area,

W = final I-region thickness (dictated by V_B),

K = permittivity,

ϵ = dielectric constant

leads one to the correct mask dimension to be used during fabrication. Since the capacitance is specified at -20 volts it is desirable that the depletion region punch through at voltages much less than this bias. A relationship can be derived using an abrupt junction approximation relating the bias voltage, depletion layer width, and background concentration. This relation is given below:

$$C_B = \frac{2K_s \epsilon_o V_{(PT)}}{qW^2}$$

We can refer to the bias voltage as the punch-through voltage in this case, and W as the punched through depletion layer width. C_B is the background concentration in atoms/cc. We can tabulate, for various background concentrations and assumed punch through voltages, the amount of spread of the depletion region, so as to arrive at the optimum starting resistivity. This data is presented in Table A-5 (assume lightly doped n-type material).

TABLE A-5.

CASE - I: Zero Bias Punch-Through

Resistivity	Doping Concentration	Atoms (Parts/ Billion)	Depletion Layer Width (Microns)
500 ohm·cm	1.3×10^{13} atoms cc	0.2	7.4
200 ohm·cm	2.5×10^{13}	0.5	5.3
100 ohm·cm	5×10^{13}	1	3.8
50 ohm·cm	1×10^{14}	2	2.7
5 ohm·cm	1×10^{15}	20	0.8

CASE - II: 2 Volt Punch-Through

Resistivity	Doping Concentration	Atoms (Parts/ Billion)	Depletion Layer Width (Microns)
500 ohm·cm	1.3×10^{13} atoms cc	0.2	15.4
200 ohm·cm	2.5×10^{13}	0.5	11.1
100 ohm·cm	5×10^{13}	1	7.9
50 ohm·cm	1×10^{14}	2	5.5
5 ohm·cm	1×10^{15}	20	1.7

Usage of the above table (or better, similar data plotted with W as a parameter) indicates that the higher resistivities are necessary for reasonable depletion layer widths at low voltages. Since the breakdown voltage of a PIN diode is related to the 'I' region impurity concentration, as well as thickness, the voltage breakdown specification will set a minimum final thickness, and the punch-through voltage

determines a minimum resistivity. The maximum electric field for high resistivity silicon is approximately 33 volts/micron. Using the relationship for an abrupt junction -

$$E_{max} = \frac{2 V_B}{W}$$

one can arrive at the conclusion that to support a 50-volt breakdown, a minimum 3.4 microns of intrinsic region is necessary. Reviewing the preceding tables concerning V_{PT} (especially if we were dealing with a difficult R_s specification where low punch through is necessary), we observe that 100 ohm·cm is the minimum resistivity which would allow zero bias punch through, and 50 ohm·cm would suffice should we be able to allow a 2-volt punch through for this V_B specification allowing for a 2.0 microns diffusion into the layer, starting material would be specified as 6 microns of 100-ohm ·cm epitaxial silicon on a heavily doped silicon substrate. A batch of 10-20 wafers is then drawn from inventory, the characteristics of layer thickness, Copeland profile, and substrate type recorded on the lot traveler. Reference is made to the epitaxial run number, date and substrate lot, so that silicon traceability is obtained. The lot arrives at the cleaning station, where the silicon wafers are subjected to solvent and acid cleansing. Organic residues, oils, dust and dirt are removed at this point; in addition, metallic contamination and organic residue from the solvent cleaner are removed. The wafers are then thoroughly rinsed in deionized water, and dried.

Immediately, the silicon wafers are loaded into boats and inserted into a high temperature oxidation furnace. Approximately 5,000 Å of thermal oxide is grown on both sides of the wafer. The wafers are withdrawn, allowed to cool in closed containers, and the oxide thickness is measured on a control wafer which accompanied the run. At this point, the process becomes different, depending on whether a planar or mesa device is desired.

The two paths differ as follows:

Planar	Mesa
Oxidized Wafers	Oxidized Wafers
↓	↓
Photolithography	Strip Oxide, High ρ side
Clean	Clean
Boron Deposit	Boron Deposit
Boron Diffusion	Boron Diffusion
	Photolithography
	Mesa Definition
	Mesa Formation

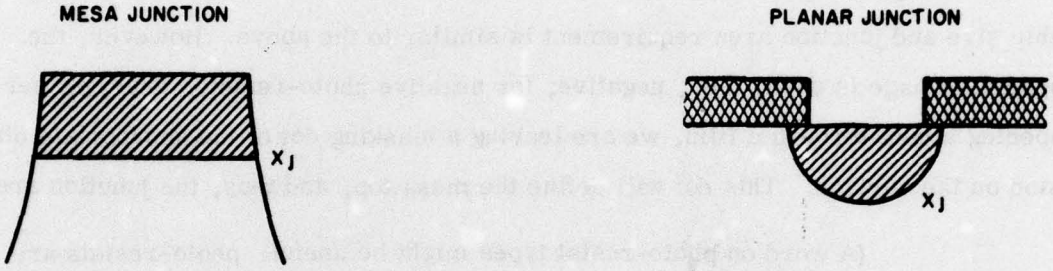
For the planar technology, the photolithographic step is determined by the junction area needed to provide the correct capacitance after diffusion and the chip size is based on package requirements, any thermal resistance considerations, and optimum packing densities on the wafers. Thus, a mask of XXX mils on YYY mil center-to-center would be ordered, and the image would be referred to as a positive mask (if negative photo result is used). The result would be a hole of XXX mil diameter and YYY mil center-to-center, cut into the thermal oxide after appropriate hydrofluoric acid etching. Each wafer would receive identical treatment, being batch processed whenever possible. Spinning and aligning, however, are individual steps and require individual wafer handling. After inspection of the wafers for appropriate dimension, and completeness of etching, as well as masking oxide integrity, the wafers are immediately cleaned and placed into the furnace for boron deposition. Times and temperatures to assure a 2-micron diffusion for this device are provided on the lot traveler. Sheet resistance controls are listed on the lot traveler, and satisfactory furnace performance is assured by measuring sheet resistance on a monitor wafer. The wafers are removed from the furnace, cooled in a closed container, and at this point are ready for their first electrical dc performance check.

In the mesa process, the masking oxide is stripped completely from the high resistivity side of the wafer. After undergoing a cleansing and rinsing operation, the wafers are dried and immediately placed into a high temperature boron deposition furnace, again with times and temperatures determined to allow a 2 micron diffusion. Sheet resistance is monitored as in the above planar process. The wafers are then removed, cooled and sent to photolithography. At this point dc statics can not be measured, as the junction extends over the entire wafer, continuously. The photo-resist application from the point of view of determining the final chip size and junction area requirement is similar to the above. However, the opposite image is used, i.e., negative, for negative photo-resist. Thus, rather than opening a hole through a film, we are leaving a masking dot of the appropriate dimension on the surface. This dot will define the mesa top, and thus, the junction area.

(A word on photo-resist types might be useful: photo-resists are referred to as positive or negative, depending on the type of interaction with ultraviolet radiation. Negative photo-resists are those which are polymerized when exposed to this radiation. Positive photo-resists are those whose polymeric chains are formed during the prebaking operation, and are broken down by the effect of ultraviolet radiation. In both cases, the nonpolymeric species is soluble in suitable solvent, while the polymeric species remains impervious to solvent action. Prolonged exposure to solvent in aqueous treatments, or standing in humid atmosphere, can affect the ability of the photo-resist to withstand these solvents, however.)

After the mesa is defined by photo-resist, it is necessary to form the mesa by silicon etching techniques. Gnerally, batch mixtures of nitric, hydrofluoric and acetic acids are used with the formulation depending on the etch depth necessary, and the etching rate desired. Since the diffusion depth is known, and the original 'I' region thickness is also known, it is only necessary to etch to a depth which ensures etching through the 'I' region, into the n^+ substrate, to prevent 'I' region exposure at the dicing operation. 'I' region exposure causes increased leakage currents paths and premature device failure. Once etching is completed, the mesa slice is now able to be probed for dc statics.

It might be noted at this point that the breakdown voltage observed for the same diffusion into similar material done by planar and mesa techniques is not the same. In the mesa situation, the junction front indeed approaches a plane junction. In the planar junction, lateral diffusion at the edges of the diffusion window results in anything but a plane junction. Thus, pictorially,



A reduced value of breakdown voltage will be observed for the planar junction because of the finite radius of curvature of the junction. Increased fields in the areas of the junction radius will cause the critical field to be reached earlier, thus breakdown will occur at those areas. This fact is normally taken into account in designing a PIN diode, when addressing the V_B specification. However, to go to a thicker 'I' region to assure higher breakdown may cause trouble in meeting capacitance or R_s specifications. Thus, the tradeoffs between device types come into play in the design aspect of the device.

At this point, similar operations are performed on either the planar or mesa device. They are listed below:

- Thermal Oxidation
- Photolithography
- Thickness Etching

- Contact Metallization
- DC Evaluation
- Dicing

Thermal oxidation is performed after boron diffusion for two reasons. Improvement of subsequent etching of the contact window by redistributing the heavy concentration of dopant at the surface, making the phase more soluble in the etchants used, is a prime consideration. Also, additional protection and stabilization of the junction is provided by additional oxide, especially where a contact will be cut in the original oxide. Generally, the temperature at which this oxidation is carried out is lower than the original cycle, so as to minimize movement of the junction. Wafers are oxidized in a batch; either standing or laying flat, in a quartz or silicon boat.

After thermal oxidation, the lot is ready for photolithography to reopen a hole or clean oxide from the top of the mesa. The contact hole must be centered within the diffusion window and must be etched completely to the silicon surface. The photo-resist layer is then stripped, and the wafers are immediately transported in closed containers to the metallization step, where they are cleaned thoroughly. Metallization consists of applying a film of metal element onto selected areas of the wafer with sufficient binding energy so that intimate contact with the heavily doped region of silicon is achieved. The contact must be "ohmic", that is to say, linear in its electrical behavior, and not add additional impedance to the device characteristics. In addition, the adhesion of the metal contact must be adequate to withstand bond pull tests as required in the specifications. Poorly made contact metallizations will show up in device performance as contact resistance, contributing to R_s (or insertion loss) increases, thermal resistance, and mechanical yield. Gold is often used as the metal to which bonding in the external circuit will be performed. Gold, however, has the chemical characteristic of forming a eutectic compound with silicon at temperatures near 300°C. Thus, a barrier metal, or metals, is necessary to prevent the silicon-gold reaction from occurring. Refractory metals fulfill this function. Techniques for

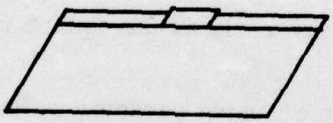
application of these metals include RF sputtering and electron beam evaporation. Each technique has its own advantages and disadvantages insofar as ease of application, adhesion characteristics, and side effects. For example, RF sputtering provides superior adhering films, but also can cause radiation damage to occur (electron-hole traps are formed in the oxide, for example). Also, step coverage in sputtered films is excellent. Electron beam evaporation (or even filament evaporation) provides a less energetic source for metal deposition, with the resultant lessening of adherence qualities. Step coverage is that expected from a point source, so that carousels and planetary action might be needed to improve this situation. Commercial vacuum systems are used in the metal deposition steps.

Vacuum is provided by either oil diffusion pumping, backed by mechanical pumps, ion-pumping, or cryo-pumping. The latter two techniques are considerably "cleaner" techniques, as the oil diffusion pumping leads to the possibility of contamination of the bell jar through oil molecules backstreaming into the chamber. Often, large surface area cold traps are inserted between the oil diffusion pump and the bell jar; these are liquid nitrogen cooled, and will freeze out impurity molecules as they attempt to migrate into the chamber. Background composition within the bell jar is normally monitored by means of mass spectrometers (called residual gas analyzers) permanently attached to the system. Hydrocarbons, water vapor, nitrogen can be easily identified by their mass peaks in an analysis sample. Monitor wafers and glass slides accompany a material lot to provide adhesion, thickness, and contact resistance information, as well as establish metal-etching rates and characteristics. Specific contact resistance for many of the metals deposited on clean, heavily doped silicon, is of the order of 10^{-6} ohms·cm^2. Thus, the quality of the metal film deposition can be monitored electrically at this point by observing the actual contact resistance measured.

The wafer lot, after metallization, is sent for dc static testing, and capacitance and lifetime measurement. Voltage breakdown, forward voltage, and, where possible, leakage current are measured at this point. In addition, capacitance voltage relations are determined (measured usually at 100 MHz) and minority carrier

lifetime is determined. Production approval for the lot is given when the above parameters are within the desired specification. Wafers are rejected if any parameter falls out of specification, as there is no recovery technique available at this stage. Approval or rejection is generally on a wafer-to-wafer basis, rather than the entire lot.

The final step in the chip fabrication is the dicing operation. Wafers are mounted by some means (either wax, vacuum, freeze-down) on an appropriate dicing system. This may be a diamond scribing machine, a diamond saw, or a laser scribing machine. These have the purpose of separating the individual chips of the correct dimension from the wafer. Diamond scribing generally involves applying a stress front into the wafer by means of a diamond-stylus and then in a subsequent step fracturing the wafer which breaks down the crystalline planes. For < 111 > type material, scribed chips have the cross sectional shape of a parallelogram, i.e.,



showing the cleavage of the wafer along the planes. On the other hand, sawed chips and laser scribed chips are rectangular in cross section, which demands different handling in subsequent automatic die mounting equipment.

Laser scribing is a relatively new technique, where the silicon is vaporized by a high intensity laser beam which is indexed along the wafer. A protective coating is applied to the wafer prior to scribing, to prevent contamination and laser "splash" from degrading the electrical performance. This protective coating, as well as any waxes or adhesives used for mounting and holding the wafer must be removed by a series of organic solvent cleansing of the chips, in combination often with ultrasonic vibration. One must be careful, however, of introducing mechanical damage by the ultrasonic treatment, and must use appropriate power levels. For that matter, mechanical damage can be introduced during any of the three above mentioned dicing operations, leading to raggedness, chipping and microcracks, which will eventually cause device failure during life testing. The scribed, cleansed chips are then placed in a sealed container and a sample is run for mechanical and electrical

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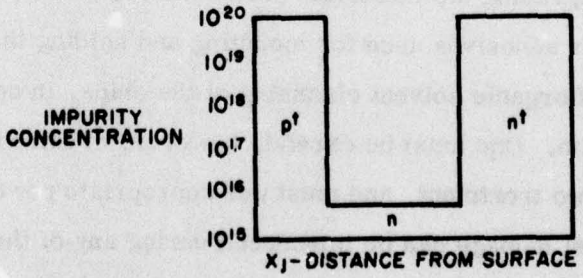
yield, to include RF testing where necessary. Resistance, switching speed, total capacitance, and voltage breakdown determine the nature of the diode; as in most microwave circuitry, however, the actual proof is the circuit performance of the diode. Often, a small difference in lifetime from lot-to-lot, or a slightly greater leakage current from lot-to-lot, could cause the device not to perform optimally in the circuit, despite the fact that the DC and RF specifications were met. Many times, explanations of this behavior can be found in terms of slightly different parasitics, bond wire length, package capacitance, etc., when the real reason is found within the chip itself. The degree of control necessary to assure high yield from slice to chip to circuit performance has not been available to date, despite the many controls presently used.

b. Tuning Varactor - As the name implies, a tuning varactor is a variable capacitance, nonlinear element; the capacitance varies as a function of applied bias voltage, ideally inversely as the square root of the applied voltage.

The fabrication of tuning varactor wafers at many steps in the process is similar to the above discussed process for the PIN wafer. The difference lies mainly in the use almost solely of the mesa construction, the difference in the starting material epitaxial layer, and the shape and magnitude of the capacitance-voltage relationship. The doping profile of a tuning varactor wafer can be shown to be the following:



As shown, we have a $p^+ - n - n^+$ structure, when n in the epitaxial layer is in the order of 1 ohm·cm. Here, much care is used in the depositing of the doped epitaxial layer, in that significant operational performance differences will be observed for differences in the first decimal place of resistivity; thus 0.8 to 1.2 ohm·cm represents doping concentrations of 7×10^{15} to 4.5×10^{15} atoms·cc and 2 ohm·cm represents 2.5×10^{15} atoms·cc. This threefold difference in doping concentration affects breakdown voltage and capacitance/area for these devices and thus must be as precisely identified as possible to design a tuning varactor to the highest figure of merit (Q factor). Thus, the diode chip must be designed such that breakdown occurs close to, but not as, the depletion layer punches through so as to leave no unswept resistive layer within the epitaxial layer. Punch through of the depletion layer cannot be allowed at a lesser bias voltage because of capacitance swing and tuning considerations. Many tuning varactors are operated near breakdown voltage so that "over-designing" from a layer thickness and V_b point of view is not possible, as this technique would serve to decrease the Q factor. The layer is then specified so as to provide optimum V_B, square-law variation of capacitance with applied bias voltage, in the correct capacitance range, on a low resistivity substrate. For example, we might specify a 5-micron, 0.8 ohm·cm (7×10^{15} atoms·cc) to be grown. This doping concentration would provide us with a voltage breakdown of 74 volts. Assuming a 2-micron diffusion we would be left with 3 microns of epitaxial material, having calculated that at this breakdown voltage and doping concentration, the epitaxial layer thickness should be about 3 microns from the relationship.

$$W = \sqrt{\frac{2K, \epsilon_0 V}{q C_B}}$$

$$= 3.4 \times 10^3 \sqrt{\frac{V_{total}}{C_B}}$$

The capacitance is usually specified at -4 volts so that the capacitance per area can be calculated at this bias voltage, which then defines the mean diameter and function area necessary to provide this capacitance. For example, the wafer is described

would have a capacitance per area of 0.07 pF/mil^2. Thus, a mesa or junction area of approximately 70 mil^2 would be needed for a tuning varactor having a capacitance of 5 pF at -4 volts.

Processing the wafers then becomes, stepwise, similar to the mesa PIN process. Thermal oxidation, followed by oxide stripping of the epi side, 3-micron boron deposit and diffusion, at an intermediately high temperature would take place. The junction should be as abrupt as possible to allow square-law behavior of the C-V characteristic. Surface concentration and substrate concentration have to be high enough (virtually degenerate material) to allow negligible contact resistance to be observed. Excessive contact resistances could also degrade Q. Q is defined as:

$$Q_{(-4)} = \frac{1}{2\pi f R_{s_{(-4)}} C_{(-4)}}$$

and contact resistance would show up in R_s.

After boron diffusion, photolithography defines the mesa by the appropriate dimension necessary for the desired capacitance at -4 volts. A positive mask is used, with negative photo-resist, leaving a dot of photo-resist whose dimension defines the mesa.

By means of a silicon etch, the mesa is now etched into the silicon, and capacitance and voltage breakdown are monitored as the etching proceeds. When the desired value at the bias voltage is obtained, the wafers are cleaned and thermally oxidized for passivation. Photolithography again clears the oxide from the mesa top. The wafer is thinned to an appropriate thickness for later dicing, and metallized on both sides. After a final dc check for V_B, V_f, and the C-V characteristic is determined, the wafer is either approved for dicing or rejected. Approved dice are evaluated on a sample basis for V_B, C-V, and Q is measured (usually at 100 MHz). Everything which was said earlier relative to dice cleanliness and surface condition is equally important for tuning varactor chip fabrication. Surface contamination or unwanted charges in the thermal oxide passivation can lead to tuning difficulties, post-tuning drift, instability or degradation of breakdown voltage and lower Q values.

In short, the surface condition of either a PIN or varactor chips is equally important from an operational point of view.

A.1.4 Traceability and Test Points

During the processing of microwave semiconductor devices, traceability and complete history of each event that occurs affecting the starting silicon material is very difficult. Equally difficult are the chemical and electrical evaluations at each step in the process, which could indicate the success or failure of a particular process step. It follows, therefore, that failure of a device in a circuit, or in a life test prior to insertion in a circuit, is not traceable as to the cause or possible process step where a latent failure mode was incorporated. The present program then has as a goal the capability of establishing as total and complete a historical record as possible, so that by improved and monitored controls and tests throughout the process, yield information is directly obtained and a correlation made with measured impurity types and levels.

Presently in a typical production area, traceability for the silicon itself is probably quite good. Thus, ingot and substrates are identified and coded; doping levels (resistivity) and dopant type are well identified. In some cases, bulk lifetime has been measured and recorded for the ingot. Likewise, the silicon epitaxial layer can be well characterized electrically and dimensionally. Resistivity, by four-point probe methods, Copeland profiling and/or differential capacitance measurements for doping concentration as a function of layer thickness, infrared reflectance, or angle lapping and staining for layer thickness are all available and much used techniques. Processes for cleaning, polishing and slicing are usually well documented as to dates, procedures, times, temperatures, and operators. A glaring weakness: since chemicals and gases are often batch mixed, delivered by long lines through flow meters, or heated in beakers, usually in open air, chemical lots and purity levels are lost and do not form part of the historical base. This weakness cannot be blamed on the chemical or gas supplier: they purify their chemicals and gases to the levels specified. However, they do not guarantee anything about

homemade receipts for batch processing and mixing chemicals. Often the chemicals are mixed in open air, in beakers which have been cleansed in the same chemicals, and rinsed in deionized water, the analytical content of which is not continuously known; or monitored. Although chemicals are usually delivered from the suppliers with lot numbers assigned, rarely does the lot number become part of the recorded history for the device manufactured, and in fact, it becomes rather meaningless when two or three types of acids are mixed, as in the silicon etches. Gases, likewise, are delivered in cylinders whose history is probably unknown. Analytically, the gas has been characterized after pressurizing the cylinder. Impurities desorbing from the cylinders, or entering from reactive materials or leaks in delivery lines and connections, flow meters, presently go unidentified and undetected, being hidden in the yield of that process step.

Once wafers begin the fabrication part of the process, traceability becomes much less. Although lot cards list processes, dates, and operator identifications, wafers constantly interact with other lots of wafers, large batches of mixed chemicals, different lots of gases, and gas mixtures, quartzware which has been cleansed in other mixtures of similar chemicals, so that conventional historical recording only scratches the surface. The hypothesis is that if the silicon is maintained under the most controlled conditions, the ambient clean and constant in humidity and temperature, the proper techniques used (with the best chemicals and gases available, in high purity quartz containers), and the design engineers knowledgeable to "hit" the specification, that the yield from wafers into devices shipped should be at least constant (although low). The processing requirements mentioned above, however, add considerable manufacturing cost to these devices because of the high capital investment necessary to provide the proper environment and high materials costs because of the extreme purity necessary in the chemicals, gases and other materials. And yet the production yields typically are no greater than 7 to 8%.

The objective of this program is to realize the next order of magnitude of control, monitoring subtrace impurity levels and all other physical and chemical

parameters which could result in improved yields through better insights into the processes based on quantitative data. The improved yields should impact government spending in these areas by lower costs per unit.

A.1.5 Failure Mode Analysis

Failure mode identification, diagnosis and prognosis are, of course, three essential elements of corrective engineering. Accordingly, we will present, in this subsection, analytical comments on key modes of failure affecting semiconductor devices. In each case we will point out the distinguishing feature of the failure mode under study.

A.1.5.1 Breakdown Voltage Degradation - This mode of failure exhibits itself as a reduction in the ultimate breakdown voltage capability of the device. We distinguish, here, those causes where catastrophic "shorts" occur within the device. The tuning varactors in particular suffer from such degradation. A PIN diode's breakdown voltage is limited mainly by the I-region thickness, and the processing that the diode undergoes does not affect that thickness. We are obviously excluding here radius of curvature type limitations since such limitations are natural and hence do not constitute a failure.

In PIN diodes, if breakdown voltage degrades it is usually catastrophic. On the other hand, in a tuning varactor, as we have seen in subsection A.1.2, the breakdown mechanism is very much determined by the carrier concentration levels and, therefore, any modulation in conductivity during processing will affect breakdown voltage. The particular process step where a reduction in V_B occurs is the oxidation (passivation) step. Reduction, when it occurs, is evident when post-oxidation measurements are compared to pre-oxidation readings. Mesa structure is recommended for breakdown voltage testing as radius of curvature effects will be eliminated; of course, the necessary precaution needs to be taken when making the V_B measurements on a bare (unpassivated) junction. However, this is certainly not insurmountable for the experienced engineer who can easily identify the true avalanche region.

Breakdown voltage degradation, therefore, is a failure mode, the detection of which tells us of a process problem in the case of tuning varactors.

A.1.5.2 Leakage Current Increase - This mode of failure is not uniquely identifiable unless a "standard" is known. Namely, the leakage current, I_r. Readings in the pre-oxidation phase are not accurate due to the exposed conditions of the junction. Thus, a comparison of such readings with the post-oxidation readings does not provide a meaningful failure analysis tool. However, one can intentionally and controllably change the process conditions and then compare I_r readings at the post-oxidation step. This does provide a relative but nevertheless a comparative failure analysis tool.

Under ideal conditions (i.e., perfectly clean and undamaged silicon surface) the leakage current will be determined by a recombination-generation mechanism. This mechanism is exacerbated by various means: one is the undesired addition of contaminants into the passivation during processing. These contaminants may or may not be in a charged-ionic state which will then affect V_B in a tuning varactor. If they are not charged, then they will constitute an "alien" site in an otherwise crystalline/amorphous (Si/SiO_2) interface where they may act as additional recombination-generation sources. Another means is the "awakening" of some impurities within the bulk which become active as a recombination-generation source during processing. Usually, however, there are annealing steps which alter bulk conditions but not surface conditions. By applying such steps one can qualitatively identify contamination on the surface.

Observing leakage current close to avalanche (but not at avalanche) for a sufficiently large number of wafers after each closely controlled process step enables us to identify "trends" in process-induced surface degradation.

A.1.5.3 High Temperature Reverse Bias (HTRB) Induced Failures - HTRB-induced failures are perhaps some of the most diagnostic. At excessively high temperatures such as 200°C and at applied biases of about 90% of breakdown, the failure mechanisms become quite accelerated. The electric field is high and mobility of impurities (on the surface or in the bulk) is high. Under these stress conditions contaminants and impurities readily move.

The important thing to observe is the mode of failure that occurs in HTRB stressing. If the devices become electrical "shorts" then the most likely candidate is improper metallization or non-ideal crystalline structure under the metal layer. Metal propagation into silicon through damaged sites in the silicon will cause shorts. Such failures will occur rapidly in shallow junction devices. Prior to shorting, however, the leakage current behavior is not affected.

Leakage current in semiconductor devices should increase with temperature at a rate of approximately 10% per degree centigrade. This law is true for bulk recombination-generation mechanism. The surface component of the recombination-generation process dominates in almost all cases with no contamination on the surface. Therefore, we cannot look at the temperature variation of leakage current and hope to identify the existence of contamination on the surface. However, once a certain temperature level is reached, the leakage current of an uncontaminated device should be time-invariant. Any tendency in I_R to change with time is a clear indication of the existence of contamination. How fast this change occurs is only a measure of the level of contamination and/or its mobility at that temperature and electric field.

The usual manifestation of this kind of HTRB-induced, leakage current-oriented failure is "channeling." Although some ionic contamination will "relax" back, after HTRB, most of it will have moved irreversibly under the difference of the electric field, to cause channeling.

Channeling is a direct result of contamination and, as such, it is a unique means of identifying process problems. It should be recognized that even though existence of channeling tells us there is contamination, its absence does not tell us the opposite. Hence, "pre-HTRB" and "post-HTRB" comparison of I-V characteristics of the diode is absolutely imperative.

A.1.6 Chemical Contamination

Chemical contamination of semiconductor materials occurs intentionally or non-intentionally during the same process. Doping of a silicon ingot, epitaxial layer or diffusion layer to a certain resistivity level is an intentional introduction of

controlled amounts of impurities so as to modify the electrical nature of the silicon. Often, however, accompanying the introduction of these specified impurities, are unwanted impurities, in concentrations sufficient to provide modification of the electrical characteristics which we originally desired. Table A-6 contains a list of many of the elemental impurities which beneficially or adversely affect silicon, and the type of effect which they are thought to have.

TABLE A-6. ELEMENTAL IMPURITIES AFFECTING SILICON

CONTAMINATES WHICH DOPE SILICON, ELECTRICALLY ACTIVE	HEAVY METALS, "FAST DIFFUSERS", AFFECT LIFETIME AND V_B
Aluminum	Gold
Antimony	Iron
Arsenic	Copper
Boron	Mercury
Gallium	ALKALI METALS, AND OTHERS WHICH DIFFUSE IN SiO_2
Mercury	Sodium
Oxygen	Lithium
Phosphorus	Cesium
CONTAMINATES WHICH FORM OXIDES	Potassium
Transition Metals; e.g.,	Hydrogen Ion
Nickel	HALIDES, WHICH CHEMICALLY REACT WITH SILICON
Molybdenum	Chlorine
Palladium	Fluorine
Silver	Bromine
Tin	Iodine
Zinc	
Chromium	
Cobalt	

Generally, contamination of silicon occurs either within the crystalline lattice of the silicon itself, within the silicon dioxide protective layer on the silicon surface, or is trapped at the interface of the Si/SiO_2. With the lattice, contamination may be of a substitutional or an interstitial nature, depending on the thermal energy (i.e., temperature) which the contaminating species had acquired during ingress. Once in position and "frozen" within the structure, the effect is that local fields are set up, usually referred to as trapping centers, or recombination centers, wherein minority carriers are trapped. For example, gold has a solubility in silicon of approximately 10^{16} atoms/cc at temperatures near 1,000°C. Once gold has diffused substitutionally, it will freeze out minority carriers to a doping level which is approximately equal to the number of substitutional gold atoms, thus drastically increasing the resistivity of the silicon. Although this effect might be beneficial toward manufacturing a zero bias punch-through device, the higher resistivity of the epitaxial layer would have a detrimental effect on series resistance of the diode under forward bias, and since dissipative losses are increased by the increase in R_s, power handling of the device is degraded.

Avenues for the introduction of these contaminants into the semiconductor material appear in any step in the process, as well as from the environment and handling of the wafers.

Any of the reagents which are used have to be assured to contain metallic impurities within their specification maximums. Sodium is probably the most difficult element to exclude from the process facility and reagents. Exposure of a junction during mesa etching to acid mixtures, deionized water rinses, and ambient conditions provides a relatively easy ingress to such metallic contamination. Migration of certain elements through diffusion tube quartzware at elevated temperatures, or back streaming of airborne contamination into an oxidation tube provides not only ingress to the contaminating species, but also the temperature required to drive the contaminant into the silicon lattice or oxide film. Finally, the handling of the wafer material throughout the process by metallic, plastic, or teflon coated tweezers, vacuum pickups and carriers, as clean as they may be, has to be considered potentially damaging to the electrical performance of the wafer. Metallic

particles, within the micron dimensions, are sufficient to degrade not only wafer performance but also processing equipment. These particles can originate from worn tweezers, from joints in gas delivery lines, from being transported by gas flows, and from an abundance of other sources. These particles adhere to the surface of the wafer, and are not removed by many cleansing operations. Then at high temperatures they are driven into the lattice to provide a mechanism for device failure.

The most obvious routes for contamination to occur for silicon is through the frequent immersions of the wafers in acids, solvents, and deionized water. Silicon etching, for mesa formation, is normally carried out in mixtures of nitric, acetic and hydrofluoric acids. The particular formulation used is dependent on the etching rate and depth required. Certain formulations are also available commercially; e.g., 6-1-1 (6 parts nitric, 1 part acetic, 1 part hydrofluoric acid). The particular formulations used in-house are mixed in batches in the chemical mixing area. They are then withdrawn from stock as needed. The chemical impurity content then, for that particular lot, is unknown.

Solvent cleaning is performed with hot trichloroethylene immersions, followed by methanol and acetone rinses - oxide etching is done by hydrofluoric acid and ammonium fluoride. All acid operations are followed by rinses in cascading deionized water. Doping is performed with boron tribromide, and with phosphorous oxychloride.

The preceding named reagents are obtained from the vendor who specifies the maximums for the particular lot purchased. Emphasis is placed on the fact that the analysis is a lot analysis, and not an individual bottle analysis. After the lot has been analyzed, it is either shipped by rail car, or dispensed into individual containers through various transfer lines, and sealed, for delivery. These containers are barrels, bottles, cans and tank trucks. Analysis is not generally performed on individual containers, although samples are undoubtedly taken. Contamination or variation in levels of contamination can occur in the transfer of chemicals through the manufacturer's delivery system, despite their own controls. Examples of the types

of lot analyses reported by the vendors for selected acids, solvents and doping sources, used within Microwave Associates for their standard production processes, are given in Table A-7.

A glance at the specifications for any of these high purity chemicals shows several things: they are far from being free from foreign species; there is much room for variation of actual concentrations (within the specification) of any of the critical contaminants to silicon. Alkali metals seem to be the most difficult to remove; e.g., low sodium "MOS" grade still allows for one part per million of sodium in solution. Sodium, unfortunately, is so common that it is a prime contaminant in SiO_2 films, and causes instabilities and voltage degradation in MOS as well as microwave devices.

The types of analyses performed are also listed on the manufacturer's specification. More common wet chemical techniques such as precipitation, titration, volumetric analysis, visible and ultraviolet spectrophotometry are supplemented by the more sensitive atomic absorption and emission techniques. These techniques are generally considered to be subtrace analytical techniques and are becoming more commonly used in the analytical industry.

Water is a major chemical in the processing of semiconductors. Cleansing and rinsing operations, dilutions of acids, plating bath formulations all involve the use of high purity water. The types of filtrations and chemical reaction necessary to provide water at the highest purity has been mentioned earlier. The selected pretreatment steps are dependent on the types of ionized and nonionized species dissolved within the water. Thus, in water there are five major types of contaminants: (1) dissolved ionizable gases, e.g. ammonia and carbon dioxide; (2) dissolved nonionic gases such as oxygen; (3) organics, which include living organisms, bacteria, algae and viruses, etc.; pyrogens, or dead residue from bacterial growth and synthetics, organic and natural molecules such as hydrocarbons, oils and carbohydrates in general and the decay products of organic materials; (4) particulate matter such as dirt, sand, colloids, etc., (5) ionizable salts such as sodium, calcium, chlorides, sulphates, etc. The water is, therefore, a major source of contamination

TABLE A-7. TYPICAL MANUFACTURERS' ANALYSES

p-TYPE AND n-TYPE DOPANTS

BORON TRIBROMIDE

Boron Tribromide

ULTREX, For Dopant Use. Certificate Provided Reporting Actual Lot Analysis

BBr_3 FW 250.52

Actual Analysis Lot 331383

Non-Metallic Impurities (in ppm)	
Arsenic (As)[a]	<0.04
Nitrogen Compounds (as N)	<0.5
Phosphate (PO_4)	<0.5
Silicon (Si)[b]	0.07
Sulfate (SO_4)[c]	1
Metallic Impurities[b] (in ppm)	
Aluminum (Al)	0.007
Antimony (Sb)	<0.03
Barium (Ba)	<0.5
Bismuth (Bi)	<0.003
Cadmium (Cd)	<0.005
Calcium (Ca)	0.07
Chromium (Cr)	<0.005
Cobalt (Co)	<0.005
Copper (Cu)	0.006
Gallium (Ga)	<0.005
Germanium (Ge)	<0.005
Gold (Au)	<0.005
Iron (Fe)	0.03
Lead (Pb)	0.006
Lithium (Li)[d]	0.1
Magnesium (Mg)	0.007
Manganese (Mn)	0.002
Mercury (Hg)	<0.05
Nickel (Ni)	<0.005
Potassium (K)[d]	0.4
Silver (Ag)	<0.0005
Sodium (Na)[d]	0.6
Strontium (Sr)	<0.05
Tin (Sn)	0.006
Zinc (Zn)	<0.005

[a]By evolution and silver diethyldithiocarbamate photometry.

[b]Average value for three ampouled samples evaporated, residual boron volatilized as methyl borate, analyzed spectrographically (DC arc, indium internal standard in graphite matrix against commercial standards), reading of lines in 2450-3875 A region; key elements found absent are reported as < (less than) the detection limit.

[c]By turbidimetry in methanol-water.

[d]By atomic absorption spectrometry.

This product is sensitive to heat and light, thus, it is best stored in a refrigerated or cold room (0° C) and protected from light to reduce leaching of elements from the container and discoloration due to liberation of bromine.

Packaged under argon.

PHOSPHORUS OXYCHLORIDE

Phosphorus Oxychloride

For Dopant Use, ULTREX, Certificate Provided Reporting Actual Lot Analysis

$POCl_3$ FW 153.33

Actual Analysis Lot 407957

Non-Metallic Impurities (in ppm)	
Ammonium (NH_4)	<1
Arsenic (As)[a]	<0.04
Nitrate (No_3)	<1
Sulfate (SO_4)[b]	<1
Metallic Impurities[c] (in ppm)	
Aluminum (Al)	0.02
Bismuth (Bi)	<0.01
Cobalt (Co)	<0.02
Copper (Cu)	<0.01
Gallium (Ga)[d]	<0.02
Iron (Fe)	<0.02
Lead (Pb)	<0.02
Lithium (Li)[d]	<0.1
Magnesium (Mg)[d]	<0.1
Manganese (Mn)	0.002
Nickel (Ni)	<0.02
Potassium (K)[d]	0.3
Silver (Ag)	<0.002
Sodium (Na)[d]	<0.1
Titanium (Ti)	<0.02
Zinc (Zn)	0.02

[a]By evolution and silver diethyldithiocarbamate photometry.

[b]By turbidimetry in methanol-water.

[c]Polyvalent metals and silver by 8-quinolinol extraction, evaporation of extract, mineralization with nitric acid, and DC-arc spectrography (essentially after N. M. Kuzmin et al., Zh. Anal. Khim., 24, 429-34 (1969) (Russ.); Chem. Abstr., 74, 27136 (1969), indium internal standard in graphite matrix against commercial standards, reading of lines in 2450-3875 A region. Average of duplicate ampouled samples; elements found at or below a significant blank value are reported as less than one-third of the blank; elements found at or below a blank value near the detection limit is reported as less than the detection limit.

[d]By atomic absorption spectrometry.

TABLE A-7. TYPICAL MANUFACTURERS' ANALYSES (Contd)

ACIDS

ACETIC ACID

Low Sodium MOS Grade

Formula: CH_3COOH
Formula Wt.: 60.05

Chemical/Physical Tests	Meets ACS Specifications	
Assay (CH_3COOH)	99.9%	min
Color (APHA)	10	max
Acetic Anhydride ($(CH_3CO_2)O$)	0.01%	max
Residue after Evaporation	0.0008%	max
Specific Gravity @ 60°/60°F	1.049-1.052	
TRACE IMPURITIES IN PARTS PER MILLION (MAXIMUM)		
Aluminum (Al)	0.1	ppm
Arsenic & Antimony (as As)	0.005	ppm
Barium (Ba)	1	ppm
Boron (B)	0.05	ppm
Calcium (Ca)	1	ppm
Chloride (Cl)	1	ppm
Copper (Cu)	0.01	ppm
Heavy Metals (as Pb)	0.3	ppm
Iron (Fe)	0.1	ppm
Lithium (Li)	1	ppm
Magnesium (Mg)	1	ppm
Nickel (Ni)	0.1	ppm
Phosphorus (as PO_4)	1	ppm
Potassium (K)	1	ppm
Sodium (Na)	1	ppm
Strontium (Sr)	1	ppm
Sulfate (SO_4)	0.5	ppm
OTHER TESTS		
Dilution Test		
Substances Reducing Dichromate		
Substances Reducing $KMnO_4$	Passes ACS Tests	
Suitability for Nonaqueous Titration		

HYDROFLUORIC ACID

Low Sodium MOS Grade

Formula: HF
Formula Wt.: 20.01

Chemical/Physical Tests	Meets ACS Specifications	
Assay (HF) (by acidimetry)	48.75-49.25%	
Color (APHA)	10	max
Fluosilicic Acid (H_2SiF_6)	0.01%	max
Specific Gravity @ 60°/60°F	1.180	
TRACE IMPURITIES IN PARTS PER MILLION (MAXIMUM)		
Aluminum (Al)	0.05	ppm
Arsenic & Antimony (as As)	0.03	ppm
Barium (Ba)	1	ppm
Boron (B)	0.05	ppm
Calcium (Ca)	1	ppm
Chloride (Cl)	5	ppm
Chromium (Cr)	0.01	ppm
Copper (Cu)	0.1	ppm
Gold (Au)	0.05	ppm
Heavy Metals (as Pb)	0.1	ppm
Iron (Fe)	0.5	ppm
Lead (Pb)	0.1	ppm
Lithium (Li)	1	ppm
Magnesium (Mg)	1	ppm
Nickel (Ni)	0.1	ppm
Nitrate (NO_3)	5	ppm
Oxidizable Species (as SO_2)	2	ppm
Phosphate (PO_4)	5	ppm
Potassium (K)	1	ppm
Residue after Ignition	5	ppm
Silver (Ag)	0.1	ppm
Sodium (Na)	1	ppm
Strontium (Sr)	1	ppm
Sulfate (SO_4)	5	ppm

NITRIC ACID

Low Sodium MOS Grade

Formula: HNO_3
Formula Wt.: 63.01

Chemical/Physical Tests	Meets ACS Specifications	
Assay (HNO_3)	70.0-71.0%	
Appearance	passes ACS test	
Color (APHA)	10	max
Specific Gravity @ 60°/60°F	1.421-1.424	
Residue after Ignition	0.0002%	max
Heavy Metals (as Pb)	0.00001%	max
TRACE IMPURITIES IN PARTS PER MILLION (MAXIMUM)		
Aluminum (Al)	0.1	ppm
Arsenic & Antimony (as As)	0.005	ppm
Barium (Ba)	1	ppm
Boron (B)	0.1	ppm
Calcium (Ca)	1	ppm
Chloride (Cl)	0.09	ppm
Chromium (Cr)	0.1	ppm
Copper (Cu)	0.01	ppm
Iron (Fe)	0.1	ppm
Lithium (Li)	1	ppm
Magnesium (Mg)	1	ppm
Nickel (Ni)	0.05	ppm
Phosphorus (as PO_4)	0.2	ppm
Potassium (K)	1	ppm
Sodium (Na)	1	ppm
Strontium (Sr)	1	ppm
Sulfate (SO_4)	0.5	ppm

TABLE A-7. TYPICAL MANUFACTURERS' ANALYSES (Contd)

SOLVENTS

ACETONE

Low Sodium MOS Grade

Formula: $(CH_3)_2CO$)
Formula Wt.: 58.08

Chemical/Physical Tests

Assay ($(CH_3)_2CO$) (by GC, corrected for H_2O)	99.5%	
Color (APHA)	10	max
Residue after Evaporation	0.0005%	max
Acidity (as CH_3COOH)	0.002%	max
Alkalinity (as NH_3)	0.001%	max
Aldehyde (as HCHO)	0.002%	max
Methanol (CH_3OH) (by GC)	0.05%	max
Substances Reducing $KMnO_4$	passes test	
Water (H_2O) (by Karl Fischer titrn.)	0.5%	max
Chloride (Cl)	passes test	
Resistivity (megohm-cm)	7.0	min

TRACE IMPURITIES IN PARTS PER MILLION (MAXIMUM)

Aluminum (Al)	1	ppm
Antimony & Arsenic (as As)	0.01	ppm
Barium (Ba)	1	ppm
Boron (B)	0.2	ppm
Calcium (Ca)	1	ppm
Copper (Cu)	0.01	ppm
Heavy Metals (as Pb)	0.2	ppm
Iron (Fe)	0.05	ppm
Lithium (Li)	1	ppm
Magnesium (Mg)	1	ppm
Nickel (Ni)	0.01	ppm
Phosphorus (as PO_4)	0.1	ppm
Potassium (K)	1	ppm
Sodium (Na)	1	ppm
Strontium (Sr)	1	ppm

TRICHLOROETHYLENE

Low Sodium MOS Grade

Formula: $ClCH:CCl_2$
Formula Wt.: 131.39

Chemical/Physical Tests

Color (APHA)	10	max
Residue after Evaporation	0.0005%	max
Acidity (as HCl)	0.0005%	max
Alkalinity (as NaOH)	0.001%	max
Free Halogens	passes test	
Water (H_2O) (by Karl Fischer titrn.)	0.005%	max
Resistivity (megohm-cm)	0.1×10^6	min

TRACE IMPURITIES IN PARTS PER MILLION (MAXIMUM)

Aluminum (Al)	1	ppm
Arsenic & Antimony (As)	0.1	ppm
Barium (Ba)	1	ppm
Boron (B)	0.05	ppm
Calcium (Ca)	1	ppm
Chloride (Cl)	1	ppm
Copper (Cu)	0.01	ppm
Iron (Fe)	0.1	ppm
Lead (Pb)	0.1	ppm
Lithium (Li)	1	ppm
Magnesium (Mg)	1	ppm
Nickel (Ni)	0.01	ppm
Phosphorus (PO_4)	0.1	ppm
Potassium (K)	1	ppm
Sodium (Na)	1	ppm
Strontium (Sr)	1	ppm
Heavy Metals	0.1	ppm

and must be included in any control system. Listed below are examples of typical selected analyses before and after water purification. These were based on seeking contaminants which "might" be in the purified water system, with no quantitative evidence other than a period of low yields and degraded device parameters during processing. The desire for better control and more quantitative information is always strongest during those "cyclical" events when for some unknown reason, degradation of an electrical parameter is observed. This has been a common and frequently observed occurrence in the semiconductor industry. The reported value of "zero" however should not be construed as being accurate. What is indicated is that the sensitivity of the particular analytical tool did not allow detection at the subtrace levels probably present.

	Raw Water (PPM)	Purified and Polished Water (PPM)
Alkalinity, Bicarbonate	44.0	0
Alkalinity, Carbonate	0	0
Calcium	65.5	0
Chlorine	91.6	-
Dissolved Solids, Total	100.0	0
Iron	0.296	0.003
Magnesium	26.5	-
pH	6.9	6.6
Sodium	69.7	0
Sulfate	22.0	0
Turbidity, Jackson Units	12	0

Likewise, when manufacturers report higher purity levels and propose new categories of chemicals (e.g., MOS, Spectro-Grades) what they are

indicating is that a new analytical technique has moved the detection sensitivity to new levels; they can now look at their process statistically and say, for example, that although they specify sodium at 10 parts per million, that they are now sure analytically that 95 percent of the time, it runs at less than one part per million. Thus, they can lower their specification, probably raise the unit price because of the higher quoted purity and the quality of the material has not changed 95 percent of the time. The occasional 5 or 10 parts per million batch however can now analytically be rejected and recycled for increased purity.

Other facts of semiconductor processing include contamination from airborne particles, particulate matter in gas lines, metallic chips, dust and handling, all of which have been mentioned earlier. Any proposed control system must have as part of its capability the technique for qualitative and quantitative analysis of these species. The process engineer then can make valid judgments about filtration, purification, types of transfer lines and the general environment in which the semiconductor devices are processed.

Finally, in considering the effects of impurities on the semiconductor device performance, it is necessary to know the concentration as well as the type of impurity, to relate this to the device's electrical performance. Furthermore, even though one may know reasonably accurately the type and concentration of an impurity in a reagent used in wafer processing, what has to be determined in any yield correlation is the actual amount of impurity within the semiconductor. It is important to determine, then, the transfer ratio for each impurity. The transfer ratio can be thought to be an equilibrium ratio of concentrations of impurity in the bulk silicon (or on the surface of silicon) to that concentration in the solution. Part of this program therefore will be to establish these coefficients, so as to predict quantitatively the effect of an impurity species introduced at a particular process step.

A.1.7 Effects of Contamination on Microwave Semiconductor Devices

As was discussed in subsection A.1.5, contamination has several forms. The process-introduced surface contamination could be ionic (as is most often the case) or nonionic. When it is ionic it will most likely be of positive polarity

and therefore it will affect the tuning varactors with n-type epi (which means almost all tuning varactors) by reducing V_B. The reduction comes about as a result of conductivity modulation in the epi. Positive charge will attract electrons to the surface causing an accumulation region there. Hence, the effective resistivity on the surface is reduced, causing a drop in the breakdown voltage capability. Such a drop, as we have stated earlier, will not occur in a PIN diode since V_B is limited by epi thickness. However, an inverse form of PIN will be affected by positive charge to the first order. This form is the NIP structure with the I-region being of π type. The surface charge, attracting electrons, will invert the surface. The inversion layer will immediately exhibit a channel in the I-V characteristics. Consequently, it is quite efficacious to use NIP diodes to detect ionic charge.

A PIN diode is still useful as a tool to detect ionic contamination. In this case, however, the forward resistance-forward current behavior must be observed and analyzed. From the relationship:

$$R_F = \frac{W_I^2}{2\mu I_F}$$

R_F-I_F curve will give us τ. Since contamination will affect lifetime a pseudo-quantitative method is thus provided to "sense" contamination.

When the contamination is nonionic there are other ways the device is affected. The degree and the nature by which the device degrades depend on the quantity and type of contamination. An undesired impurity, when introduced onto the silicon surface at some point along the process, will move into silicon at a later point when high temperature processing occurs. This could be during diffusion, oxidation, metallization or even assembly. These impurities after moving into silicon will act like traps increasing the recombination-generation probability. The net result is a decrease in lifetime. For a tuning varactor the decrease in lifetime will not be easy to measure because, in general, the process does not have an "anneal-slow cool" step to bring the native lifetime up. In the absence of such an anneal step the lifetime even with no contamination is low. It is not expected to go down measurably lower unless a catastrophic contamination occurs.

However, the indirect effect is a degradation in V_B and/or leakage current. For a PIN or NIP, the lifetime will be measurably lowered and so lifetime testing should be an integral part of contamination detection.

Ionic or nonionic contamination will influence the rate and manner of failures in HTRB stressing. As pointed out in subsection A.1.5, observation of channeling will disclose contamination. Also, time variation in leakage current will disclose contamination.

There is another phenomenon which is drastically affected by surface contamination: post tuning drift (PTD). Since the frequency stability of a microwave system is adversely affected, post tuning drift has attracted much attention lately. The motion of surface charges in a tuning varactor causes a change in capacitance - sometimes very minutely - after a step in voltage. Qualitatively, it has been found that two types of such charges may be present. One type has a short time constant and will give rise to an overshoot in the capacitance charge (ΔC) at room temperature. The other type has a longer time constant and results in a lagging capacitance response.

Sometimes it may be possible to make these effects partially cancel each other but the apparently positive result is deceptive. The reason is that the two effects have a substantially different temperature dependence and, therefore, compensation is possible at one temperature only. The tuning varactor processing must, as a consequence, aim at eliminating surface contamination even when V_B, I_R and HTRB testing give acceptable results.

In summary, we have at our disposal several electrical measurement methods such as V_B readings, I-V characteristics observations, lifetime measurements and HTRB testing to tell us about the existence and relative degree of extent of contamination acquired during processing. Combined with spectroscopic analysis, all these measurement techniques will provide a powerful tool to identify and take corrective action against contamination.

APPENDIX B

INSTRUMENTATION SELECTION

B-1 GENERAL

There are a great many types of analytical instruments available today for measuring elements in very low concentration, and continuing improvements in their performance are steadily lowering their limits of detectability. Many instrumental methods are capable of microgram and nanogram limits, while selected methods have demonstrated picogram (10^{-12}g) and femtogram (10^{-15}g) limits. The more commonly used chemical analysis techniques are listed as follows:

a.	Mass Spectrometry: • Electron Impact • Spark Source • Ion Probe • Chemical Ionization	Detects all elements. Instrumentation is generally complex and expensive.
b.	Neutron Activation	Detects all elements. Instrumentation is often expensive. Control and disposal of irradiated samples may present a problem.
c.	Atomic Absorption Spectrometry	Detects about 60 elements. A source is specific to each element.
d.	Atomic Emission Spectrometry	Detects all elements. A particular instrumentation may be limited by physical constraints upon the number of detectors which can be mounted.
e.	X-Ray Fluorescence	Detects elements with atomic numbers above 11.

f.	Anodic Stripping Voltametry	Detects about 20 elements.
g.	Surface Analysis: • ESCA • ISS • Auger • SIMS	Detects and identifies atoms in first several atomic layers of a surface. Among the most sensitive methods known.
h.	Ion-Selective Electrodes	Sensitivity depends upon the element and electrodes.

Since it must be assumed that all 35 contaminating elements may be present at any time it will be generally necessary to measure all of them. It would be preferable therefore to select instruments that are sensitive to a broad spectrum of elements rather than ones which are specific. It is anticipated that a great many specimens will have to be tested, so preference will be given in the selection to instruments which are capable of making simultaneous measurements. Naturally, among the considerations in choosing a method of analysis is what information is sought. Elemental identification, possibility of chemical reaction (e.g. corrosion), compound identification (e.g., residual gas), visual observation, concentration of a species as a function of depth or area (e.g., mono-atomic surface layers) might all be of interest. Among the techniques available for specimen excitation are electron beams, X-ray beams, photons (lasers), neutron beams, ultrasonic and ion beams. Generally, these beams can be focused and excitations can be observed. Among these excitations are secondary electrons, characteristic X-rays, sputtered ions, Auger electrons, scattered ions, photoelectrons. These excitations (which also can be focused and separated or detected either by mass or energy) will depend on the energy of the exciting beam for their detectability as well as the atomic number of the element excited. Some of the analytical methods are listed below:

METHOD	DETECTION LIMITS (gms)
X-Ray Fluorescence	10^{-7}
Transmission Electron Microscopy (TEM)	
Electron Spectroscopy for Chemical Analysis (ESCA)	10^{-9}
Emission Spectroscopy	10^{-15}

METHOD	DETECTION LIMITS (gms)	
Ion Sputtering Spectroscopy (ISS)	10^{-11}	
Nuclear Backscattering	10^{-12}	High Z on low Z substrate
Mass Spectrometry	10^{-13}	
Electron Probe Microanalysis (EPMA)	10^{-15}	
Auger Spectroscopy	10^{-16}	10Å of surface
Secondary Ion Mass Spectroscopy (SIMS)	10^{-18}	

In terms of the applicability of the methods:

	SURFACE ($\sim$ 100 Å)	BULK
For Area Localization:	1. SIMS	1. ES/TEM
($\sim$ 100 μ)	2. Auger	2. SIMS
In order of decreasing sensitivity	3. Low Voltage EPMA	3. EPMA
		4. Auger
		5. Emission Spectroscopy
For Broad Beam Analysis:	1. SIMS	1. SIMS
In order of decreasing sensitivity	2. Auger	2. Mass Spectroscopy
	3. Nuclear Back-scatter	3. Emission Spectroscopy
		4. Nuclear Activation
		5. Auger

An example of the sample size and the detection limits for several of the above techniques are given below:

	SAMPLE ANALYZED	DETECTABILITY	COMMENTS
EPMA	10^{-10} gms	10^{-4} -10^{-5}	Best quantitative method
Auger	10^{-13} gms	10^{-3}	Good surface, poor bulk

	SAMPLE ANALYZED	DETECTABILITY	COMMENTS
SIMS	10^{-12} gms	10^{-4} -10^{-6}	+ions, -ions, quantitative not easy
TEM	10^{-18} gms	10^{-2}	Low atomic number Thin samples

Since these techniques are among the most recently developed and sensitive, some comments about the basis for analysis and some relative comparisons are appropriate. Generally speaking, quantitative or qualitative analysis can be performed within the bulk of the material, near the surface, or on the surface. Bulk techniques generally include liquid and gaseous (as well as solid) phases, while surface analysis generally must be performed on solid materials.

For surface techniques, to determine elemental species, we have available: X-Ray Energy Dispersion, Auger Spectroscopy, Electron Spectroscopy for Chemical Analysis (ESCA), Ion Microprobe Microanalysis (IMMA), Ion Sputtering Spectroscopy and Secondary Ion Mass Spectrometry (ISS, SIMS) as well as others. Let us consider some of the properties of these techniques:

a. Auger Spectroscopy: Excitation by X-ray or electron beam ejects an electron from the K-shell leaving a hole; an electron from the L-shell fills the hole and a second L-shell electron is emitted which is the Auger electron. The energy can be given:

$$KE = E_K - 2E_L \text{ (shell energies)}$$

and can be measured, and peaks in the detector (scintillator) can be correlated to atoms on the surface. The Auger electron is detectable within 10 Å of the surface. All elements for $Z>3$ can be measured, while helium is difficult and H_2 is not possible. An ion beam can then be used to sputter away an amount of the layer and the next 10 Å can be analyzed, so that a "depth" profile can be accomplished. Applications and examples include thin metal film interactions, migration reactions with O_2 (poor contact resistance), gold Auger imaging (is gold there, or missing?), aluminum-silicon alloying, Pt-Si tungsten gold system, boron doped polysilicon for gate technology and metal adherence problems.

b. ESCA (Electron Spectroscopy for Chemical Analysis): Involves an energy analysis of secondary electrons; one can also couple this technique with ion sputtering for depth analysis. ESCA is a large area analysis (e.g., 1 mm as opposed to 0.2 micron for Auger) and its depth is greater than Auger (as least twice as deep). ESCA has different surface sensitivities than Auger, and thus can be used to complement Auger. An example of an application is the investigation of silicon rich thermal oxide (not completely oxidized, pin holes, scratches, etc.). The Auger would merely show the peaks for silicon and oxygen, with no information on compound information.

c. Ion Microprobe Microanalysis (IMMA): The exciting species can be ions of oxygen, argon or nitrogen. All elements can be detected to the levels of parts per billion. The area can be as small as 1 to 2 microns depending on beam focus. Although this technique is commercially available, there are fewer than 20 in the US. A 50-angstrom depth resolution is possible. After excitation the primary ion is detected and either recorded, ion-imaged or ion-counted. There are problems in interpreting the information from this technique due to cratering, wall effects. Thus rastering of the beam within the crater is necessary, increasing equipment expense. In addition, quantitative analysis is most difficult. This technique allows elemental identification from hydrogen to uranium, isotopic identification and chemical analysis over small areas.

d. Ion Sputtering Spectroscopy and Secondary Ion Mass Spectrometry (ISS, SIMS): The exciting beam in this technique is an ion beam, usually a noble gas. The atoms to be analyzed are those heavier than the noble gas used. The exciting species loses energy (upon collision) which is directly related to the mass of the surface atom. The following table shows some advantages of ISS, and also of the SIMS technique which is a further refinement:

ISS

Advantages	Disadvantages
Surface sensitive	Sputtering does occur
Spectra are simple	Poor resolution of adjacent atoms
Sensitive to heavy atoms	No light atoms

ISS (Contd)

Advantages	Disadvantages
Insulators and hydrocarbons analyzable	Charge exchange
No matrix effects	Crater and edge effects

SIMS

Advantages	Disadvantages
Mass resolution	No quantitative
Detection of H and He	Ionization effects vary
Sensitive to light atoms	Not surface sensitive

Some applications of the above techniques include metal film analysis, polymer films, plating problems, mechanism of oxide growth on thin films and multilayer metallization for magnetic memory disks.

The general characteristics of the above techniques can be summarized as follows: they present in logical fashion the ability to arrive at the mechanism of failure of devices to a degree never before possible. They generally are very expensive, time-consuming techniques. Sample preparation is often painstakingly slow, and contamination of the data is very easy. Significant capital expense would be incurred for even the basic SEM, although there are units available for $25K to $35K. To enable the SEM to be used for other applications, the cost starts to climb prohibitively (EDAX, Auger, etc.). There are companies whose sole existence is the analysis of failures using these techniques. Thus, it almost becomes necessary to conclude that the more complex analytical techniques should be sought only when absolutely necessary (because of cost) and that the experiment be designed to maximize the information to be obtained, at the most economical level. Furthermore, these techniques are for the most part used after the failure has occurred, rather than as a real-time, in-process capability, and, as mentioned earlier, they are primarily restricted to surface or near surface analysis.

Various types of instruments differ widely in the time required to make a measurement. Some require lengthy and meticulous sample preparations. Some, like a gas chromatograph, exhibit significant processing times. Others require lengthy cleaning and purging procedures after each sample. For example, some

neutron activation analyzers require expensive installations or, as the proton NMR some are extremely expensive. In selecting the analytical instruments for this program the dominant criterion will be "total cost per element ensemble."

For bulk analysis, with the capability of both liquid and gaseous determinations, an initial survey of the techniques available indicates that atomic emission spectroscopy provides the range of elemental determination necessary, the real-time analytical capability coupled with the sensitivity level demanded.

At the present time, then, a plasma coupled emission spectrometer of the type manufactured by Jarrell-Ash (Jarrell-Ash Plasma Atomcomp, Cat. No. 96-975) or its equivalent is found to most economically fit the technical needs of the program.

The general selection, however, of emission spectroscopy over any of the above techniques, is justified as the initial critical point in an in-process control and monitoring system. To be able to know contamination levels quantitatively before a semiconductor slice has been processed, and to know the critical contaminants and their threshold levels, can have a far more effective impact on improved yields and lower manufacturing costs than many of the far more expensive tools which are more applicable to failure analysis. These systems however, can be later incorporated into an overall control and monitoring system for real-time surface analysis, although that does not fall within the scope of the present program.

B-2 SYSTEM INSTALLATION

Upon selection of the designated analytical tool, the selected instruments will be procured, modified and adapted where necessary and installed in the microwave semiconductor facilities of Microwave Associates, Inc., Burlington, Massachusetts. There the instruments will be used to perform a series of controlled experiments designed to establish the transfer ratios for the analytic model, to monitor the contamination levels in an operating semiconductor production process, and to identify the critical contaminants and their threshold values detrimental to microwave devices.

It is noted that any selection made will be thoroughly substantiated and documented giving definitive requirements, selection criteria and alternatives.

The analytic model will identify precisely the data which must be acquired, and its relevance to the project objectives. Once the data are acquired, their validity will be checked by inserting them into the analytical model to see if they produce results which are consistent with experience.

APPENDIX C

ANALYTIC MODEL DESIGN

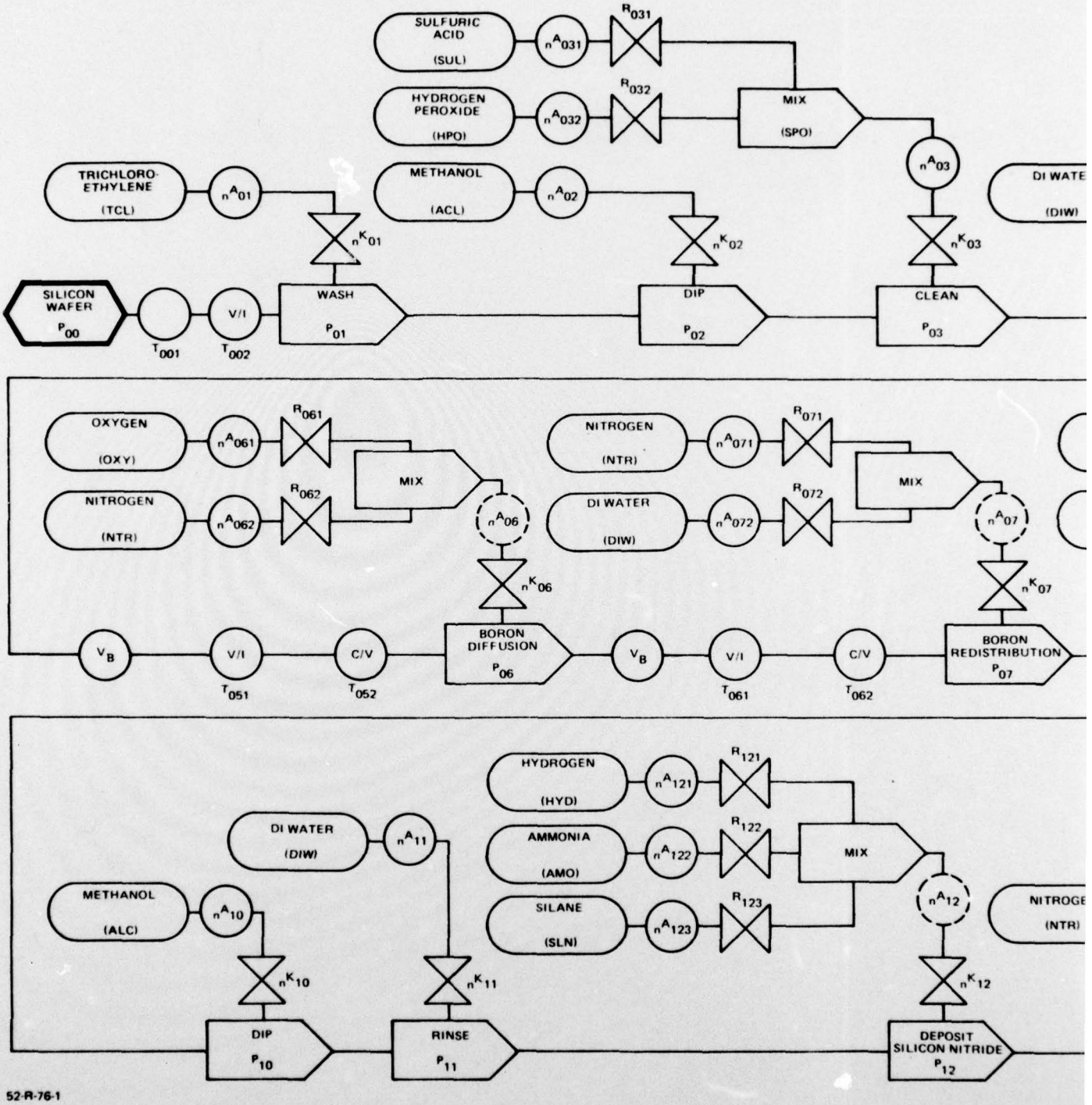
Figure C-1, PIN Diode Manufacturing Process, is a diagram of those features of the manufacturing process which are to be modeled. The process starts with a silicon wafer at process steps P_{00} and proceeds through 50 processing steps to emerge as a batch of finished diode chips ready for mounting and packaging.

Initially the wafer is characterized by a physical measurement of the average number of crystalline lattice dislocations per unit area and by a measurement of its bulk resistivity.

In the diagram, physical and electrical measurements are represented by circles, the nature of each measurement being indicated by inscribed letters and numerals. The letter A indicates a chemical analysis measuring the concentration of a contaminant. The pre-subscript n relates to the elemental chemical species, e.g., sodium, potassium, etc., and the post-subscript relates to the process step. ${}_{n}A_{m}$ is to be interpreted as the measured concentration of the chemical element n at process step m.

(Note: the notations ${}_{n}A_{m}$ and ${}_{n}K_{m}$ are wholly equivalent to the more conventional notation A_{nm} and K_{nm}. The former was chosen for greater clarity in diagramming the process).

K is a transfer function or coupling coefficient relating a measured concentration level A to the product yield Y. Being a function of both a chemical species and process step, it carries appropriate subscripts. K is not the simple numeric proportion of A entering the process but is the proportionate effect of A upon the product yield. For example, if A were to represent the concentration level of a totally innocuous element, K would assume a value of zero, even though the element might enter the process at that point in relatively large proportions. In those instances where the operation is a simple mixing process, the symbol R is used to indicate a ratio which is species non-specific.


SULFURIC ACID
(SUL)
$_nA_{031}$
R_{031}
HYDROGEN PEROXIDE
(HPO)
$_nA_{032}$
R_{032}
MIX
(SPO)
$_nA_{03}$
TRICHLORO-ETHYLENE
(TCL)
$_nA_{01}$
METHANOL
(ACL)
$_nA_{02}$
DI WATE
(DIW)
$_nK_{01}$
$_nK_{02}$
$_nK_{03}$
SILICON WAFER
P_{00}
T_{001}
V/I
T_{002}
WASH
P_{01}
DIP
P_{02}
CLEAN
P_{03}
OXYGEN
(OXY)
$_nA_{061}$
R_{061}
NITROGEN
(NTR)
$_nA_{062}$
R_{062}
MIX
$_nA_{06}$
NITROGEN
(NTR)
$_nA_{071}$
R_{071}
DI WATER
(DIW)
$_nA_{072}$
R_{072}
MIX
$_nA_{07}$
$_nK_{06}$
$_nK_{07}$
V_B
V/I
T_{051}
C/V
T_{052}
BORON DIFFUSION
P_{06}
V_B
V/I
T_{061}
C/V
T_{062}
BORON REDISTRIBUTION
P_{07}
HYDROGEN
(HYD)
$_nA_{121}$
R_{121}
AMMONIA
(AMO)
$_nA_{122}$
R_{122}
SILANE
(SLN)
$_nA_{123}$
R_{123}
MIX
$_nA_{12}$
NITROGE
(NTR)
DI WATER
(DIW)
$_nA_{11}$
METHANOL
(ALC)
$_nA_{10}$
$_nK_{10}$
$_nK_{11}$
$_nK_{12}$
DIP
P_{10}
RINSE
P_{11}
DEPOSIT SILICON NITRIDE
P_{12}

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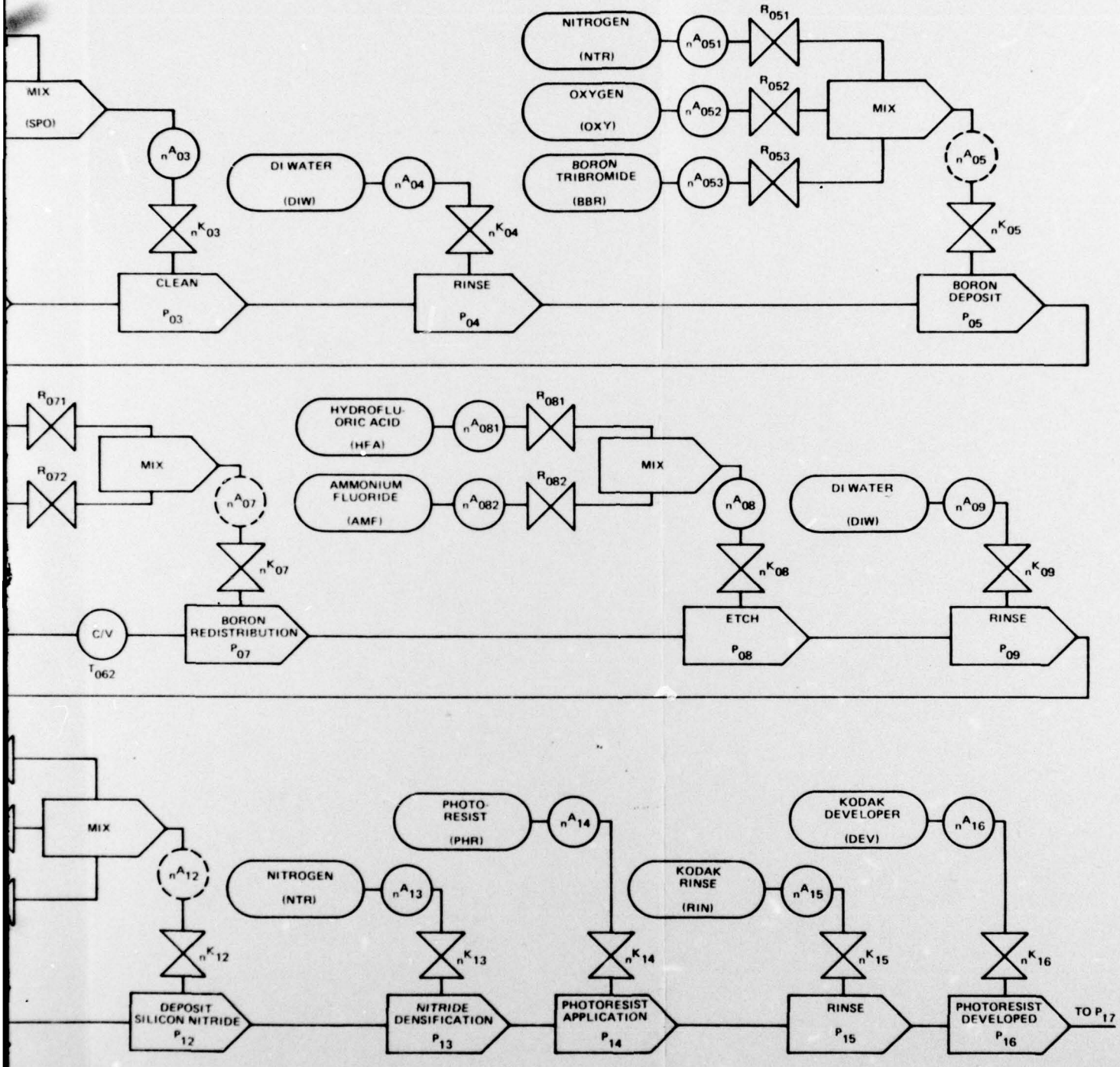
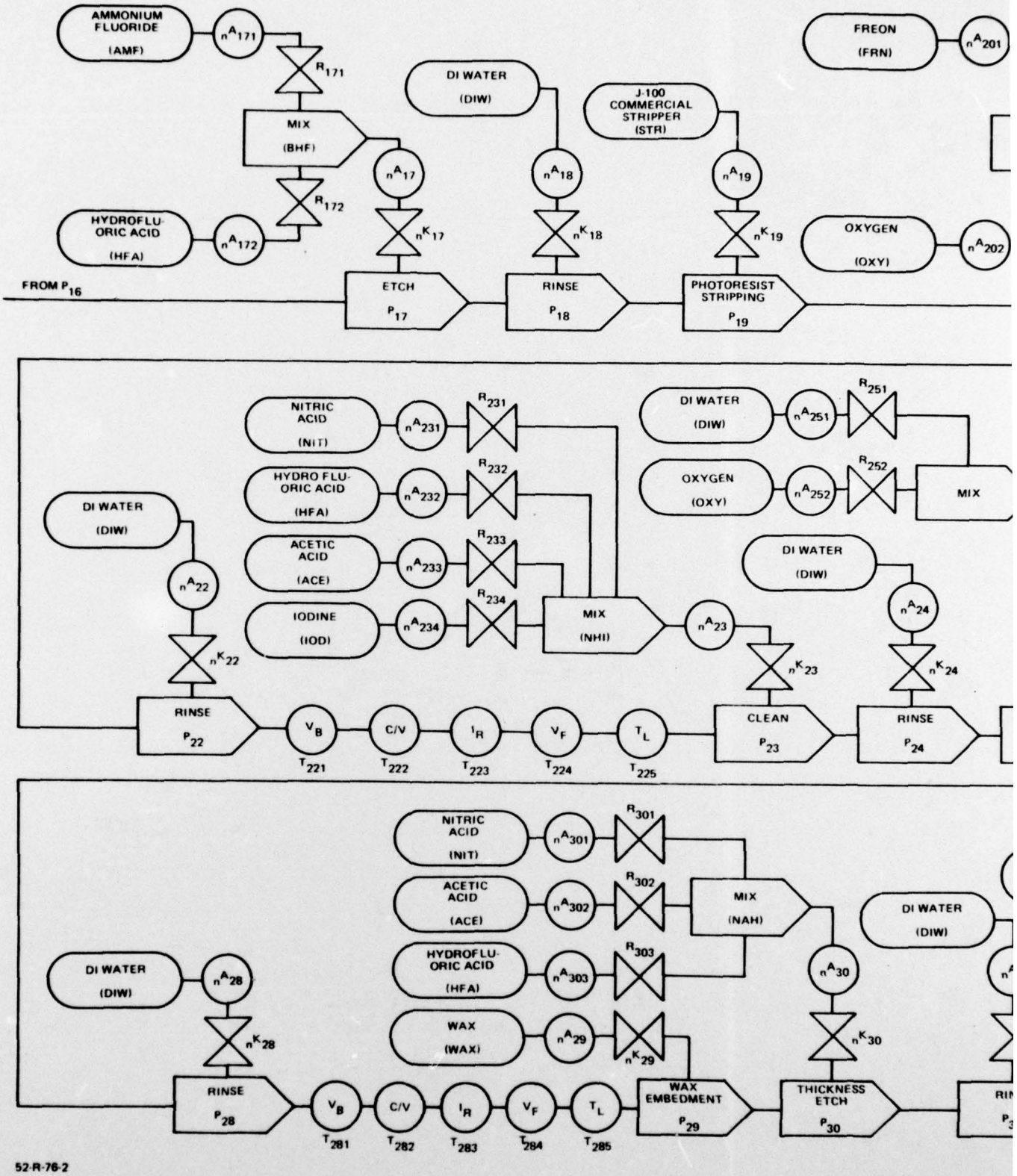


Figure C-1. PIN Diode Manufacturing Process (Sheet 1 of 3)


AMMONIUM FLUORIDE (AMF)
n^{A}_{171}
R_{171}
MIX (BHF)
R_{172}
HYDROFLUORIC ACID (HFA)
n^{A}_{172}
n^{A}_{17}
n^{K}_{17}
DI WATER (DIW)
n^{A}_{18}
n^{K}_{18}
J-100 COMMERCIAL STRIPPER (STR)
n^{A}_{19}
n^{K}_{19}
FREON (FRN)
n^{A}_{201}
OXYGEN (OXY)
n^{A}_{202}
FROM P_{16}
ETCH P_{17}
RINSE P_{18}
PHOTORESIST STRIPPING P_{19}
NITRIC ACID (NIT)
n^{A}_{231}
R_{231}
HYDRO FLUORIC ACID (HFA)
n^{A}_{232}
R_{232}
ACETIC ACID (ACE)
n^{A}_{233}
R_{233}
IODINE (IOD)
n^{A}_{234}
R_{234}
MIX (NHI)
DI WATER (DIW)
n^{A}_{251}
R_{251}
OXYGEN (OXY)
n^{A}_{252}
R_{252}
MIX
DI WATER (DIW)
n^{A}_{22}
n^{K}_{22}
n^{A}_{23}
n^{K}_{23}
DI WATER (DIW)
n^{A}_{24}
n^{K}_{24}
RINSE P_{22}
V_B T_{221}
C/V T_{222}
I_R T_{223}
V_F T_{224}
T_L T_{225}
CLEAN P_{23}
RINSE P_{24}
NITRIC ACID (NIT)
n^{A}_{301}
R_{301}
ACETIC ACID (ACE)
n^{A}_{302}
R_{302}
HYDROFLUORIC ACID (HFA)
n^{A}_{303}
R_{303}
WAX (WAX)
n^{A}_{29}
n^{K}_{29}
MIX (NAH)
DI WATER (DIW)
n^{A}_{28}
n^{K}_{28}
n^{A}_{30}
n^{K}_{30}
DI WATER (DIW)
RINSE P_{28}
V_B T_{281}
C/V T_{282}
I_R T_{283}
V_F T_{284}
T_L T_{285}
WAX EMBEDMENT P_{29}
THICKNESS ETCH P_{30}
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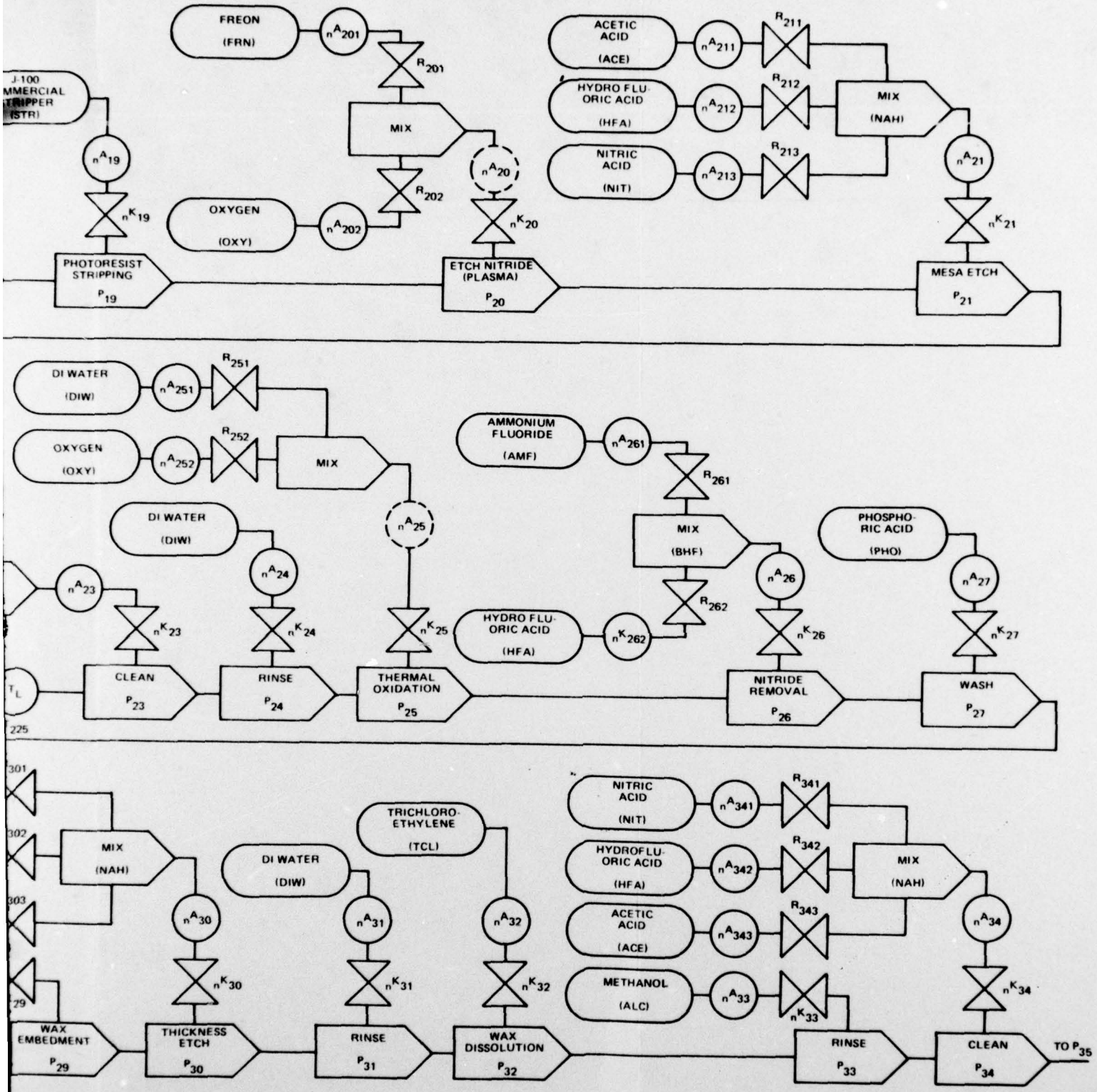
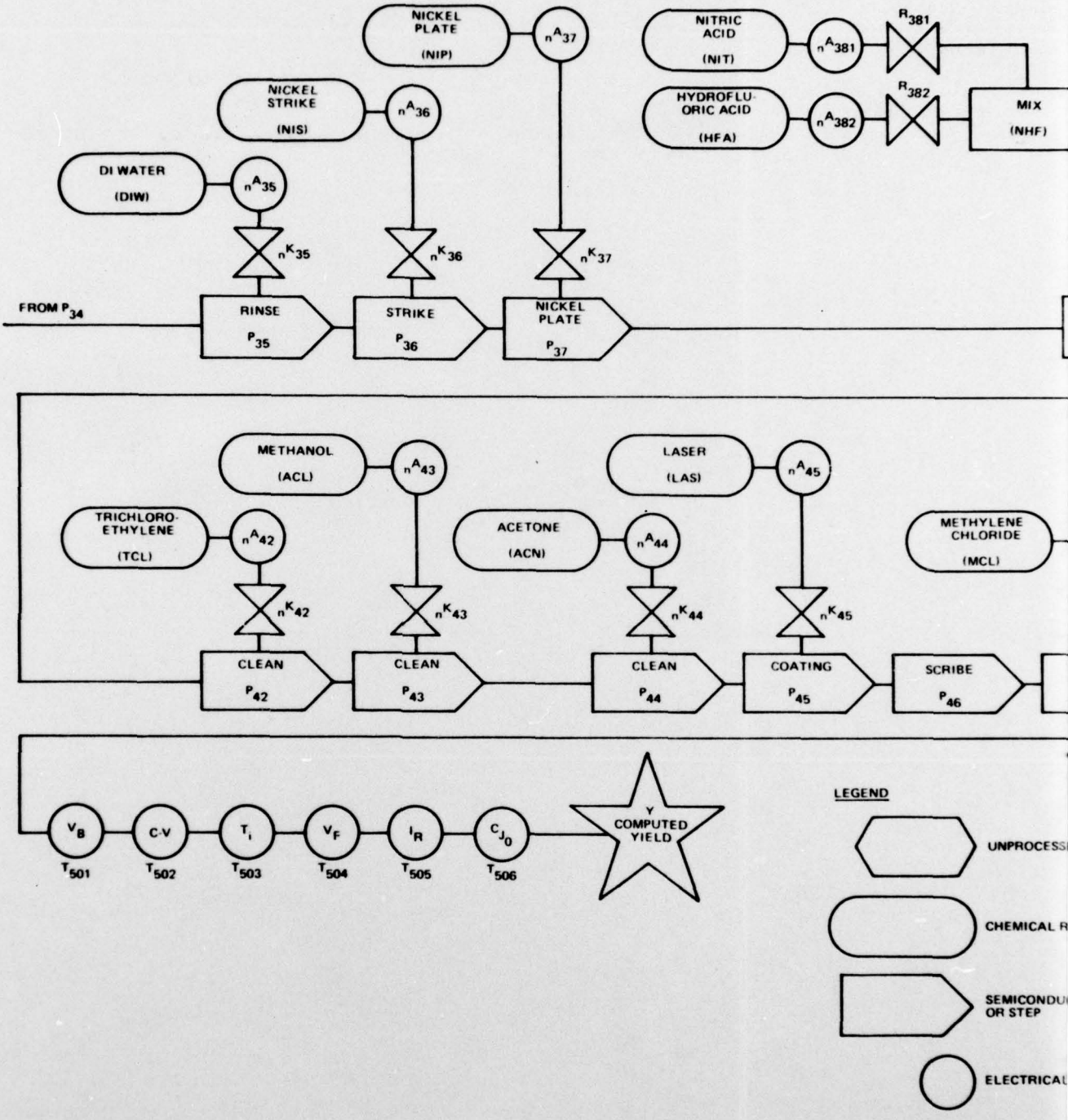


Figure C-1. PIN Diode Manufacturing Process (Sheet 2 of 3)


NICKEL PLATE (NIP)
$_nA_{37}$
NICKEL STRIKE (NIS)
$_nA_{36}$
DI WATER (DIW)
$_nA_{35}$
$_nK_{35}$
$_nK_{36}$
$_nK_{37}$
FROM P_{34}
RINSE P_{35}
STRIKE P_{36}
NICKEL PLATE P_{37}
NITRIC ACID (NIT)
$_nA_{381}$
R_{381}
HYDROFLUORIC ACID (HFA)
$_nA_{382}$
R_{382}
MIX (NHF)
METHANOL (ACL)
$_nA_{43}$
LASER (LAS)
$_nA_{45}$
TRICHLOROETHYLENE (TCL)
$_nA_{42}$
ACETONE (ACN)
$_nA_{44}$
METHYLENE CHLORIDE (MCL)
$_nK_{42}$
$_nK_{43}$
$_nK_{44}$
$_nK_{45}$
CLEAN P_{42}
CLEAN P_{43}
CLEAN P_{44}
COATING P_{45}
SCRIBE P_{46}
V_B T_{501}
C-V T_{502}
T_i T_{503}
V_F T_{504}
I_R T_{505}
C_{J_0} T_{506}
Y COMPUTED YIELD
LEGEND
UNPROCESS
CHEMICAL R
SEMICONDU OR STEP
ELECTRICAL

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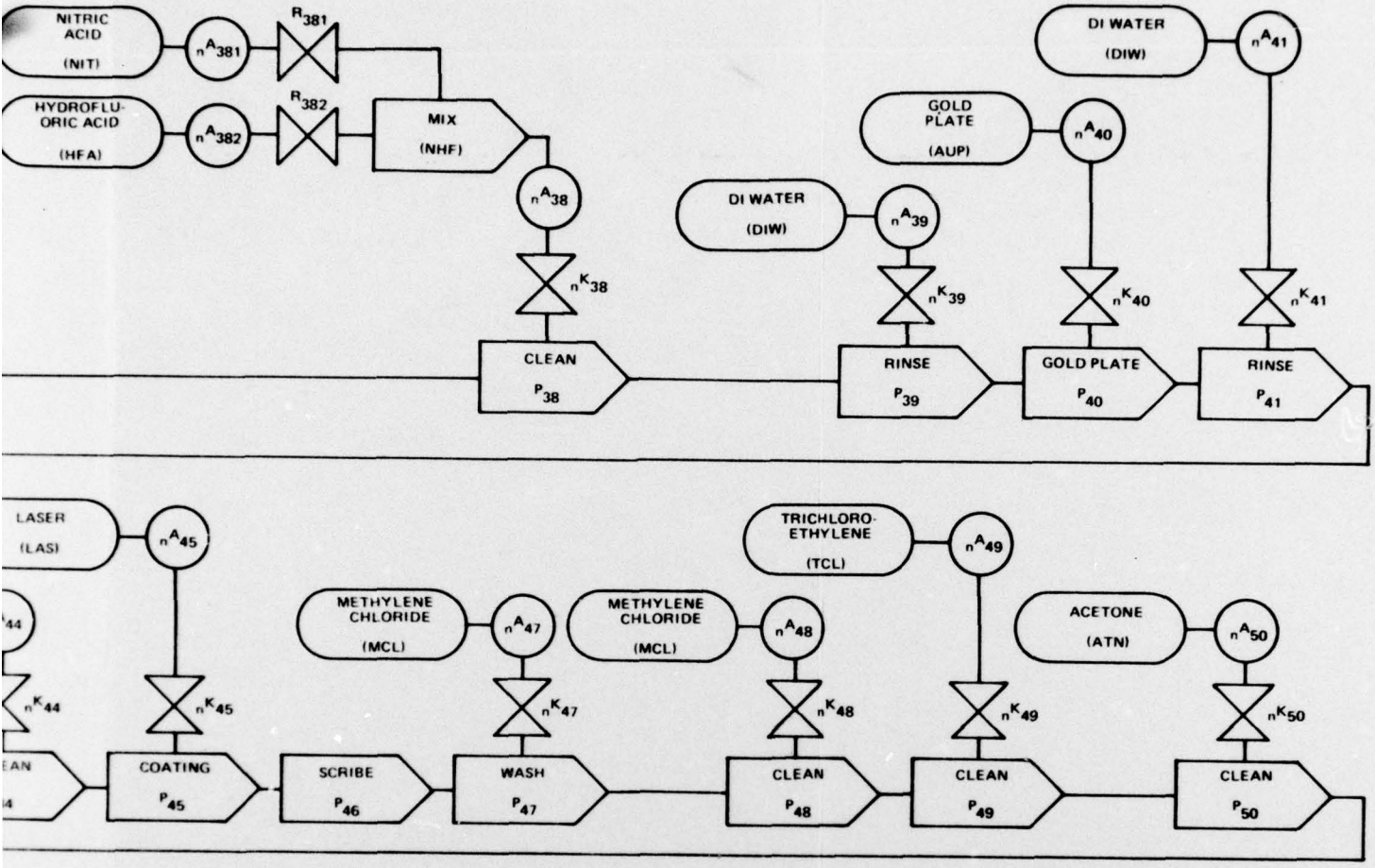

LEGEND

UNPROCESSED SILICON WAFER

CHEMICAL REAGENT

SEMICONDUCTOR PROCESSING OPERATION OR STEP

ELECTRICAL, PHYSICAL OR CHEMICAL MEASUREMENT

COMPUTED OR DERIVED INDIRECT MEASUREMENT

TRANSFER RATIO OR COUPLING COEFFICIENT

P_{XX} - PROCESS STEP IDENTIFICATION

T_{XX} - ELECTRICAL TEST IDENTIFICATION

A - MEASURED OR DERIVED CONTAMINANT CONCENTRATION LEVEL

K - VALUE OF TRANSFER RATIO

ELEMENTAL SPECIES — $_nA_m$, $_nK_m$ — PROCESS STEP

Figure C-1. PIN Diode Manufacturing Process (Sheet 3 of 3)

The process will be modeled by programming the relationships described by equations in Figures C-2 through C-4. In Figure C-2, ${}_nA_m$ may assume either measured values or, in certain specific cases, computed values. Those values which are computed will be in accordance with the relationships described in Figure C-3, Ancillary Processes. The chemical and physical similarities between elemental species will be modeled as represented by Figure C-4, Relative Effectivity, wherein ${}_nB$ represents the relative effectivity of the species.

The elements to be modeled are:

n = 1 - Aluminum (Al)
2 - Antimony (Sb)
3 - Arsenic (As)
4 - Boron (B)
5 - Bromine (Br)
6 - Cadmium (Cd)
7 - Calcium (Ca)
8 - Carbon (C)
9 - Cesium (Cs)
10 - Chlorine (Cl)
11 - Chromium (Cr)
12 - Cobalt (Co)
13 - Copper (Cu)
14 - Fluorine (F)
15 - Gallium (Ga)
16 - Germanium (Ge)
17 - Gold (Au)
18 - Iodine (I)
19 - Iron (Fe)
20 - Lead (Pb)
21 - Lithium (li)
22 - Magnesium (Mg)
23 - Manganese (Mn)
24 - Mercury (Hg)
25 - Molybdenum (Mo)
26 - Nickel (Ni)
27 - Oxygen (O)
28 - Valladium (Pd)
29 - Phosphorus (P)
30 - Potassium (K)
31 - Rubidium (Rb)
32 - Silver (Ag)
33 - Sodium (Na)
34 - Tin (Sn)
35 - Zinc (Zn)

For the purpose of the model and the data processing it will support, it is to be assumed that measurements will be made to an accuracy of one percent over a range of 10^5, i.e., a minimum of 1,157 resolvable elements for each measurement.

$$\sum_{j=001}^{002} L_j T_j + \left(\sum_{n=1}^{35}\sum_{m=01}^{05} {}_nA_m\,{}_nK_m\right)\left(1 + \sum_{j=051}^{052} L_j T_j\right) + \left(\sum_{n=1}^{35} {}_nA_{06}\,{}_nK_{06}\right)\left(1 + \sum_{j=061}^{062} L_j T_j\right) + \left(\sum_{n=1}^{35}\sum_{m=07}^{22} {}_nA_m\,{}_nK_m\right)\left(1 + \sum_{j=221}^{225} L_j T_j\right) + \left(\sum_{n=1}^{35}\sum_{m=23}^{28} {}_nA_m\,{}_nK_m\right)\left(1 + \sum_{j=281}^{285} L_j T_j\right) + \left(\sum_{n=1}^{35}\sum_{m=29}^{50} {}_nA_m\,{}_nK_m\right)\left(1 + \sum_{j=501}^{506} L_j T_j\right) + K_o = -\text{LOG } y$$

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Figure C-2. Baseline Process Equation

(2.1) $_nA_{03} = {}_nA_{031}\,R_{031} + {}_nA_{032}\,R_{032}$

(2.2) $_nA_{05} = {}_nA_{051}\,R_{051} + {}_nA_{052}\,R_{052} + {}_nA_{053}\,R_{053}$

(2.3) $_nA_{06} = {}_nA_{061}\,R_{061} + {}_nA_{062}\,R_{062}$

(2.4) $_nA_{07} = {}_nA_{071}\,R_{071} + {}_nA_{072}\,R_{072}$

(2.5) $_nA_{08} = {}_nA_{081}\,R_{081} + {}_nA_{082}\,R_{082}$

(2.6) $_nA_{12} = {}_nA_{121}\,R_{121} + {}_nA_{122}\,R_{122} + {}_nA_{123}\,R_{123}$

(2.7) $_nA_{17} = {}_nA_{171}\,R_{171} + {}_nA_{172}\,R_{172}$

(2.8) $_nA_{20} = {}_nA_{201}\,R_{201} + {}_nA_{202}\,R_{202}$

(2.9) $_nA_{21} = {}_nA_{211}\,R_{211} + {}_nA_{212}\,R_{212} + {}_nA_{213}\,R_{213}$

(2.10) $_nA_{23} = {}_nA_{231}\,R_{231} + {}_nA_{232}\,R_{232} + {}_nA_{233}\,R_{233} + {}_nA_{234}\,R_{234}$

(2.11) $_nA_{25} = {}_nA_{251}\,R_{251} + {}_nA_{252}\,R_{252}$

(2.12) $_nA_{26} = {}_nA_{261}\,R_{261} + {}_nA_{262}\,R_{262}$

(2.13) $_nA_{30} = {}_nA_{301}\,R_{301} + {}_nA_{302}\,R_{302} + {}_nA_{303}\,R_{303}$

(2.14) $_nA_{34} = {}_nA_{341}\,R_{341} + {}_nA_{342}\,R_{342} + {}_nA_{343}\,R_{343}$

(2.15) $_nA_{38} = {}_nA_{381}\,R_{381} + {}_nA_{382}\,R_{382}$

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Figure C-3. Ancillary Processes Equation

(3.1) $_{21}B_{21}K_m = {}_{33}B_{33}K_m = {}_{30}B_{30}K_m = {}_{31}B_{31}K_m = {}_{9}B_{9}K_m$

(3.2) $_{22}B_{22}K_m = {}_{7}B_{7}K_m$

(3.3) $_{11}B_{11}K_m = {}_{25}B_{25}K_m$

(3.4) $_{26}B_{26}K_m = {}_{28}B_{28}K_m$

(3.5) $_{13}B_{13}K_m = {}_{32}B_{32}K_m = {}_{17}B_{17}K_m$

(3.6) $_{35}B_{35}K_m = {}_{6}B_{6}K_m = {}_{24}B_{24}K_m$

(3.7) $_{4}B_{4}K_m = {}_{1}B_{1}K_m = {}_{15}B_{15}K_m$

(3.8) $_{16}B_{16}K_m = {}_{34}B_{34}K_m = {}_{20}B_{20}K_m$

(3.9) $_{29}B_{29}K_m = {}_{3}B_{3}K_m = {}_{2}B_{2}K_m$

(3.10) $_{14}B_{14}K_m = {}_{10}B_{10}K_m = {}_{5}B_{5}K_m = {}_{18}B_{18}K_m$

(3.11) $_{11}B_{11}K_m = {}_{23}B_{23}K_m = {}_{19}B_{19}K_m = {}_{12}B_{12}K_m = {}_{26}B_{26}K_m = {}_{13}B_{13}K_m = {}_{35}B_{35}K_m$

(3.12) $_{25}B_{25}K_m = {}_{28}B_{28}K_m = {}_{32}B_{32}K_m = {}_{6}B_{6}K_m$

(3.13) $_{17}B_{17}K_m = {}_{24}B_{24}K_m$

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Figure C-4. Relative Effectivity Equation

The model will be implemented in such a form that, as data on the process are gathered, a system of simultaneous non-homogeneous linear algebraic equations will be generated which can be solved by established algorithms.